Application Report
SPRABI2B—March 2012

# Hardware Design Guide for KeyStone I Devices

*High-Performance and Multicore Processors*

## Abstract

This document describes hardware system design considerations for the KeyStone family of processors. This design guide is intended to be used as an aid during the development of respective application hardware. Other aids including but not limited to device data sheets and explicit collateral should also be used.

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## Purpose

This document is intended to aid in the hardware design and implementation of a KeyStone I-based system. This document should be used along with the respective data manual and other relevant user guides and application reports.

## Trademarks

SmartReflex is a trademark of Texas Instruments.
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## Terms and Abbreviations

| | |
|---|---|
| AIF | Antenna Interface |
| AMI | IBIS Algorithmic Modeling Interface |
| BGA | Ball Grid Array |
| CML | Current Mode Logic, I/O type |
| Data Manual | Also referred to as the Data Sheet |
| DDR3 | Double Data Rate 3 (SDRAM Memory) |
| DSP | Digital Signal Processor |
| EMIF | External Memory Interface |
| FC-BGA | Flip-Chip BGA |
| GPIO | General-Purpose I/O |
| I2C | Inter-IC Control Bus |
| IBIS | Input Output Buffer Information Specification, or ANSI/EIA-656-A |
| IO | Input / Output |
| JEDEC | Joint Electronics Device Engineering Council |
| LJCB | Low Jitter Clock Buffer: Differential clock input buffer type, compatible with LVDS & LVPECL |
| LVDS | Low Voltage Differential Swing, I/O type |
| McBSP | Multi-Channel Buffered Serial Port |
| MDIO | Management Data Input/Output |
| NSMD | Non-Solder Mask Defined BGA Land |
| OBSAI | Open Base Station Architecture Initiative |
| PCIe | Peripheral Component Interconnect Express |
| PHY | Physical Layer of the Interface |
| PTV | Process / Temperature / Voltage |
| RIO | Rapid IO, also referred to as SRIO |
| Seating Plane | The maximum compression depth of the BGA for a given package design |
| SerDes | Serializer/De-Serializer |

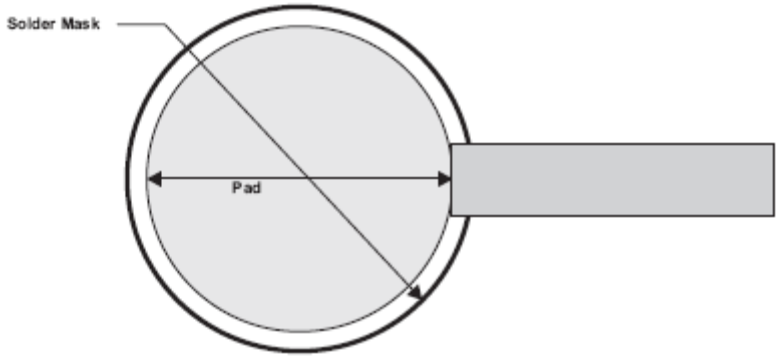
| | |
|---|---|
| SGMII | Serial Gigabit Media Independent Interface |
| SPI | Synchronous Serial Input/Output (port) |
| SRIO | Serial RapidIO |
| TBD | To Be Determined. Implies something is currently under investigation and will be clarified in a later version of the specification. |
| UART | Universal Asynchronous Receiver / Transmitter |
| UI | Unit Interval |
| XAUI | 10 Gigabit (X) Attachment Unit Interface standard |

# 1 Mechanical

## 1.1 Ball Grid Array (BGA) Layout Guidelines

The BGA footprint and pin escapes can be laid out as defined in *Flip Chip BGA Users Guide* (SPRU811) [15]. If the DDR3 interface is used, there are specific recommendations for the BGA pad and pin escape vias given in *DDR3 Design Requirements for KeyStone Devices* (SPRABI1). Given the 0.80 mm-pitch, it is recommended that non-solder-mask-defined (NSMD) PCB lands be used for mounting the device to the board. With the NSMD method, the land area is etched inside the solder mask area. While the size control is dependent on copper etching and is not as accurate as the SMD method, the overall pattern registration is dependent on the copper artwork, which is quite accurate. The trade-off is between accurate dot placement and accurate dot size. NSMD lands are recommended for small-pitch BGA packages because more space is left between the copper lands for signal traces. Dimensioning for the pad and mask are provided in *Flip Chip BGA Users Guide* (SPRU811) [15].

**Figure 1 Non-Solder-Mask Defined (NSMD) PCB Land**




## 1.2 Thermal Considerations

Understanding the thermal requirements for the C66x device along with proper implementation of a functional thermal management scheme is necessary to assure continued device performance and reliability. Each application, platform, or system must be designed to assure that the maximum case temperature of the device never exceeds the allowable limit (refer to the respective data manual for thermal requirements, limitations, and operating ranges) identified. Proper heat dispersion can be obtained using a variety of methods; including heat sinks.

**Note—**Improper thermal design that results in thermal conditions outside the allowable range will decrease device reliability and may cause premature failure.

### 1.2.1 Heat Transfer

There exist several methods for meeting the thermal requirements of the device, the two most common methods are conduction and convection.

#### 1.2.1.1 Conduction

Conduction heat transfer refers to the conduction or direct contact between two surfaces resulting in a thermal transfer from one surface (higher temperature) to another (lower temperature). When referring to the cooling of the device in an application/system this usually involves the direct contact of a heat sink (attached or

possibly part of the system enclosure). The heat generated by the device is transferred to an attached heat sink/outer enclosure thereby reducing the heat (conducting it away) on the device. In all conduction methods, the material used, compression forces, and ambient temperatures affect the transfer rates.

#### 1.2.1.2 Convection

Convection refers to the thermal transfer of heat from one object (e.g., DSP) to the ambient environment typically by means of air movement (e.g., fan). Convection or air movement can be pulled or pushed across the device depending on the application. If a fan is attached to the device the direction is usually to force the air away from the device where as if the system or application board includes external cooling fans the air direction can be either direction (push or pull). Air movement in any enclosure involves a plenum whether intended or not, it is always best to optimize the air movement to maximize the effects and minimize any excessive back pressure on the fan (to maximize fan life and minimize noise).

## 1.3 KeyStone I Power Consumption

The KeyStone I processor can consume varying amounts of power depending heavily on usage, implementation, topology, component selection, and process variation. Refer to the respective TI power application brief for early power estimations, and the respective power application note and spreadsheet for more detailed configurations and more accurate power figures.

**Note—**All numbers provided (in product briefs and app notes) assume properly designed power supplies and proper implementation of the recommended variable core (SmartReflex) supply.

## 1.4 System Thermal Analysis

For an overview on performing a thermal analysis and suggestions on system level thermal solutions, refer to the Thermal Design Guide for KeyStone Devices (SPRABI3).

## 1.5 Mechanical Compression

Mechanical compression, especially where conduction cooling is concerned (Section 1.2.1.1) is important. Excessive compression may improve thermal transfer but also increases the risk of damage to the device or inducing added electrical shorts between BGA balls on the application hardware. Excessive mechanical compression is typically noted when using BGA sockets or interfacing a heat sink/enclosure in direct contact with the device. See the data sheet and all relevant application notes regarding mechanical compression and BGA assembly.

The following tables are provided as assistance for applications where conductive cooling is utilized and a mechanical compression heat sink is incorporated. The following data assumes an absolute maximum solder ball collapse of 155 µm, 0.8 mm solder ball pitch, 841 pins, and uniform pressure across the entire device lid, a 23 mm × 23 mm lid, and proper device assembly to the PCB.

**Table 1 Maximum Device Compression - Leaded Solder Balls**

| | Maximum Lid Pressure for Leaded Ball - 0.8mm pitch (841 ball package) | | | |
|---|---|---|---|---|
| TEMP | 5 years | 10 years | 15 years | 20 years |
| 70° C | 108.67 psi | 90.59 psi | 81.57 psi | 75.69 psi |
| 90° C | 73.20 psi | 61.00 psi | 54.90 psi | 50.83 psi |
| 100° C | 61.00 psi | 75.69 psi | 45.64 psi | 42.47 psi |

**Table 2 Maximum Device Compression - Lead-Free Solder Balls**

| | Maximum Lid Pressure for Lead Free Ball - 0.8mm pitch (841 ball package) | | | |
|---|---|---|---|---|
| TEMP | 5 years | 10 years | 15 years | 20 years |
| 70° C | 544.47 psi | 447.32 psi | 397.62 psi | 365.99 psi |
| 90° C | 442.80 psi | 363.73 psi | 323.06 psi | 298.21 psi |
| 100° C | 402.14 psi | 329.84 psi | 293.70 psi | 271.10 psi |

**Note—**The values provided in the above two tables are *Not To Exceed* estimates based on modeling and calculations - added safety margin should be included to account for variations in PCB planarity, solder mask, and thermal conductive material between the DSP and compression heat sink.

# 2 Device Configurations and Initialization

On KeyStone I devices, boot modes and certain device configuration selections are latched at device reset via specific pins, which may be multiplexed with general-purpose I/O (GPIO) pins or other pins. In addition to these inputs, some peripheral usage (enabled/disabled) may also be determined by the peripheral configuration registers after DSP reset. Most of the peripherals on KeyStone I processors are *enabled* after reset; however, some are by default configured as *disabled*. The basic information on configuration options, boot modes options and use of the power configuration registers can be found in the appropriate KeyStone I data manual.

## 2.1 Device Reset

The C66x device can be reset in several ways. The methods are defined and described in greater detail in the data manual. The KeyStone I device incorporates four external reset pins and one reset status pin: $\overline{\text{POR}}$, $\overline{\text{RESET}}$, $\overline{\text{LRESET}}$, $\overline{\text{RESETFULL}}$, and $\overline{\text{RESETSTAT}}$ respectively. Additional reset modes are available through internal registers, emulation, and a watchdog timer. Each of the reset pins ($\overline{\text{POR}}$, $\overline{\text{RESET}}$, $\overline{\text{LRESET}}$, $\overline{\text{RESETFULL}}$) must have a correct logic level applied at all times (cannot be floating or in a metastable condition).

**Note—**Refer to the data manual for specific device reset requirements.

### 2.1.1 $\overline{\text{POR}}$

$\overline{\text{POR}}$ is an active low signal that must be asserted during device power-up to reset all internal configuration registers to a known good state. Additionally $\overline{\text{POR}}$ must be asserted (low) on a power-up while the clocks and power planes become stable. Most output signals will be disabled (high-impedance) while POR is low.

During a $\overline{\text{POR}}$ condition, $\overline{\text{RESET}}$ should be de-asserted before POR on power-up, otherwise the device comes up in the warm reset condition.

Proper $\overline{\text{POR}}$ utilization is required and must be configured correctly. Refer to the device data manual for additional $\overline{\text{POR}}$ details.

The internal $\overline{\text{POR}}$ circuit is unable to detect inappropriate power supply levels including power supply brown-outs. It is necessary that all power supplies be at valid levels (stable) prior to the release of $\overline{\text{POR}}$. The use of power good logic in the controlling $\overline{\text{POR}}$ circuitry reduces the risk of device degradation due to power failures. Power good logic can re-assert $\overline{\text{POR}}$ low when a power supply failure or brown-out occurs to prevent over-current conditions.

### 2.1.2 $\overline{\text{RESETFULL}}$

$\overline{\text{RESETFULL}}$ is an active low signal that will reset all internal configuration registers to a known good state. $\overline{\text{RESETFULL}}$ performs all the same functions as $\overline{\text{POR}}$ and is also used to latch the BOOTMODE and configuration pins. $\overline{\text{RESETFULL}}$ must be asserted (low) on a power-up while the clocks and power planes become stable and for the specified time after $\overline{\text{POR}}$ has been released. For the timing requirements of $\overline{\text{POR}}$ and $\overline{\text{RESETFULL}}$ please see the data manual for your KeyStone I device. Once $\overline{\text{POR}}$ has been released the $\overline{\text{RESETFULL}}$ signal may be toggled at any time to place the KeyStone I device into a default state.

During a $\overline{\text{RESETFULL}}$ condition, $\overline{\text{RESET}}$ should be de-asserted before $\overline{\text{RESETFULL}}$, otherwise the device comes up in the warm reset condition.

The proper use of $\overline{\text{RESETFULL}}$ is required and must follow all timing requirements. Refer to the device data manual for additional $\overline{\text{RESETFULL}}$ details. $\overline{\text{RESETFULL}}$ and $\overline{\text{POR}}$ must be controlled separately. The KeyStone I part will not operate correctly if they are tied together.

If $\overline{\text{POR}}$ is asserted due to an incorrect power supply voltage the $\overline{\text{RESETFULL}}$ must also be asserted until the prescribed time after $\overline{\text{POR}}$ has been released to assure that the proper configuration is latched into the device.

### 2.1.3 $\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is a software configurable reset function to the device that is available either externally via a pin or internally through a MMR (memory mapped register). When asserted (active low); $\overline{\text{RESET}}$ functions to reset everything on the device except for the test, emulation and IPs that have reset isolation enabled.

When $\overline{\text{RESET}}$ is active low, all 3-state outputs are placed in a high-impedance state. All other outputs are driven to their inactive level. The PLL multiplier and PLL controller settings return to default and must be reprogrammed if required. If necessary the reset isolation register within the PLL controller can be modified to block this behavior. This setting is mandatory for reset isolation to work. For additional details on reset isolation, refer to the applicable PLL Controller Specification.

**Note—**$\overline{\text{RESET}}$ does not latch bootstrapping. The previous values latched and/or programmed into the Device Status Register remain unchanged.

### 2.1.4 $\overline{\text{LRESET}}$

The $\overline{\text{LRESET}}$ signal can be used to reset an individual CorePac or all CorePacs simultaneously. This signal, along with the $\overline{\text{NMI}}$, can be used to affect the state of an individual CorePac without changing the state of the rest of the part. It is always used in conjunction with the CORESEL inputs and the $\overline{\text{LRESETNMIEN}}$ input for proper operation. $\overline{\text{LRESET}}$ does not reset the peripheral devices, change the memory contents, or change the clock alignment. $\overline{\text{LRESET}}$ does not cause $\overline{\text{RESETSTAT}}$ to be driven low.

The $\overline{\text{LRESET}}$ must be asserted properly to function correctly. All setup, hold, and pulse width timing for the proper implementation of the $\overline{\text{LRESET}}$ can be found in the KeyStone I Data Manual for the device that you are using. For proper operation, the following steps should be implemented:

1. Select the CorePac to be reset by driving the code for that CorePac onto the CORESEL input pins. The code values can be found in the data manual for the KeyStone I device you are using.
2. Drive the $\overline{\text{LRESET}}$ input low. This can be done simultaneously with the CORESEL pins.
3. Once both the CORESEL inputs and the $\overline{\text{LRESET}}$ input have been valid for the specified setup time, drive the $\overline{\text{LRESETNMIEN}}$ input low.
4. Keep the $\overline{\text{LRESETNMIEN}}$ input low for the specified minimum pulse width time.
5. Drive $\overline{\text{LRESETNMIEN}}$ high.
6. Keep the values of CORESEL and $\overline{\text{LRESET}}$ valid for the specified hold time.

#### 2.1.4.1 Unused $\overline{\text{LRESET}}$ Pin

If the $\overline{\text{LRESET}}$ is not used, TI recommends that it be pulled high with an external resistor to ensure that the CorePacs are not unintentionally reset. (This is a recommendation, not a requirement. It adds addition noise margin to this critical input.) The $\overline{\text{LRESETNMIEN}}$ and CORESEL inputs are also used in conjunction with the $\overline{\text{NMI}}$ to send an interrupt to one of the CorePacs. If neither $\overline{\text{LRESET}}$ or $\overline{\text{NMI}}$ are used then it is recommended that the $\overline{\text{LRESET}}$, $\overline{\text{NMI}}$, and $\overline{\text{LRESETNMIEN}}$ inputs be pulled high with external resistors. The CORESEL pins can be left unconnected, relying on their internal resistors to hold them in a steady state.

### 2.1.5 Reset Implementation Considerations

The actuation of an external pin reset can occur using either an external mechanical switch or control logic. Depending on the quality of mechanical switch selected, it may be necessary to use a de-bounce circuit (Figure 2) to prevent multiple resets (switch de-bounce) from occurring in succession. A good quality mechanical switch minimizes this risk but does not always eliminate it.

The simplest and lowest cost de-bounce circuit to implement when using a mechanical switch is an RC (resister-capacitor) voltage divider circuit. A Schmitt Trigger buffer or equivalent positive feedback circuit should be added between the RC circuit and the reset input to guarantee a proper rise-time for the reset input. Slowly varying inputs are not acceptable.

**Figure 2 Reset Mechanical De-bounce Circuit**

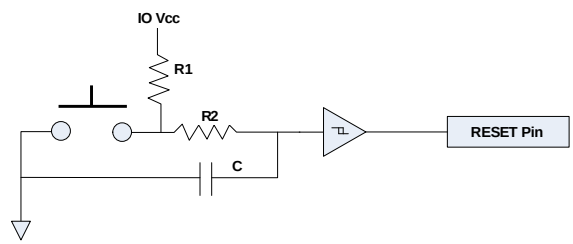



Figure 2 illustrates a recommended debounce circuit if a mechanical switch is used. To solve for R1, R2, & C we use the following formula where R equals R1 plus R2:

**Figure 3 RC Calculation Formula**

$$R = \frac{-t}{C * \ln\left(V_{th} / V_{initial}\right)}$$

Where:

- $V_{cap}$ = Voltage across the cap @ time "t"
- $V_{initial}$ = initial voltage on the cap (1.8V)
- t = time in seconds
- $V_{th}$ = worst case VT- for a SN74AUP1G17 is 1.24 V
- Let C = 1 µF

$$R = \frac{-20e^{-3}}{1.0^{-6} * \ln\left(1.24 / 1.8\right)} \qquad R = \frac{-20e^{-3}}{1.0^{-6} * \ln(0.6888889)}$$

$$R = \frac{-20e^{-3}}{1.0^{-6} * -0.372675285} \quad R = \frac{-20e^{-3}}{-373e^{-9}}$$

$$R = -20e^{-3} * -2683301104$$

$$R = 53.6K\Omega$$

Therefore, let:

- R1 = 10K ohms
- R2 = 43.6K ohms
- C = 1 µF

### 2.1.6 $\overline{\text{RESETSTAT}}$

The $\overline{\text{RESETSTAT}}$ signal indicates the internal reset state. The $\overline{\text{RESETSTAT}}$ pin is asserted low by almost all reset initiators and it remains low until the device completes initialization. The only resets that do not cause $\overline{\text{RESETSTAT}}$ to be asserted low are initiators of local CorePac reset such as the $\overline{\text{LRESET}}$. More information is available in the specific KeyStone I device data manual.

### 2.1.7 EMULATION RESET

The KeyStone I family supports the emulation reset function as part of its standard offering. Emulation reset supports both a hard and soft reset request. The source for this reset is on-chip Emulation logic. This reset behavior is same as Hard / Soft reset based on the reset requester type. This reset is non-blockable.

## 2.2 Device Configuration

Several device configuration strapping options are multiplexed with the GPIO pins (refer to data manual for proper pin assignment). There are dedicated configuration pins, such as CORECLKSEL, and DDRSLRATE1:0. The state of these pins is not latched and must be held at the desired state at all times. Refer to the Data Manual for details on the configuration options.

If the GPIO signals are not used, the internal pull-up and pull-down resistors can be used to set the input level and external pull-up/down resistors are only needed if the opposite setting is desired. If the GPIO pins are connected to other components or a test point, the internal pull-up/pull-down resistor should not be relied upon. 1k Ω pull-up and pull-down resistors are recommended for all desired settings. If multiple configuration inputs are tied together from one or more devices (recommended for input-only pins), the external resistor should have a maximum value of 1000/N where N is the number of input pins.

The phase-locked loop (PLL) multipliers can only be set by device register writes. For details on configuration of the PLL, see the KeyStone I Architecture Software-Programmable Phase-Locked Loop (PLL) Controller Users Guide (SPRUGV2) and the Data Manual.

## 2.3 Peripheral Configuration

In addition to the external device reset configuration which is covered in the previous section, there are several external configuration pins to set. These include: bit ordering (endian), PCI mode, and PCI enable. Refer to the data manual and GPIO section for correct pin configuration.

Any additional configurations not listed in this or previous sections are done through register accesses. Peripherals that default disabled can be enabled using the peripheral configuration registers. If the boot mode selection specifies a particular interface for boot (SRIO, Ethernet, $I^2C$), it is automatically enabled and configured. For additional details on peripheral configurations see the Device Configuration section in the data manual.

In some cases, the peripheral operating frequency is dependent on the device core clock frequency and/or boot mode inputs. This should be taken into account when configuring the peripheral.

## 2.4 $I^2C$ ROM Configuration Tables

The C66x device contains an $I^2C$ ROM with configuration tables: one design to provide predefined configurations used during boot and a second that allows customer defined memory map accesses during the $I^2C$ boot mode. These accesses can be used to configure peripherals during the boot process. For details, see KeyStone Architecture Bootloader User Guide (SPRUGY5).

## 2.5 Boot Modes

The C66x device contains multiple interfaces that support boot loading. These include: EMAC (Ethernet Media Access Controller), SRIO (Serial Rapid IO), PCIe (Peripheral Component Interconnect – express), Emulation, $I^2C$ (Inter-Integrated Circuit), SPI, HyperLink.

For details regarding boot modes, see the KeyStone Architecture Bootloader User Guide (SPRUGY5) and the respective KeyStone I data manual. Regardless of the boot mode selected, a connected emulator can always reset the device and acquire control.

# 3 Clocking

This section defines the key issues to consider during the hardware development for the C66x devices.

## 3.1 PLL Initialization

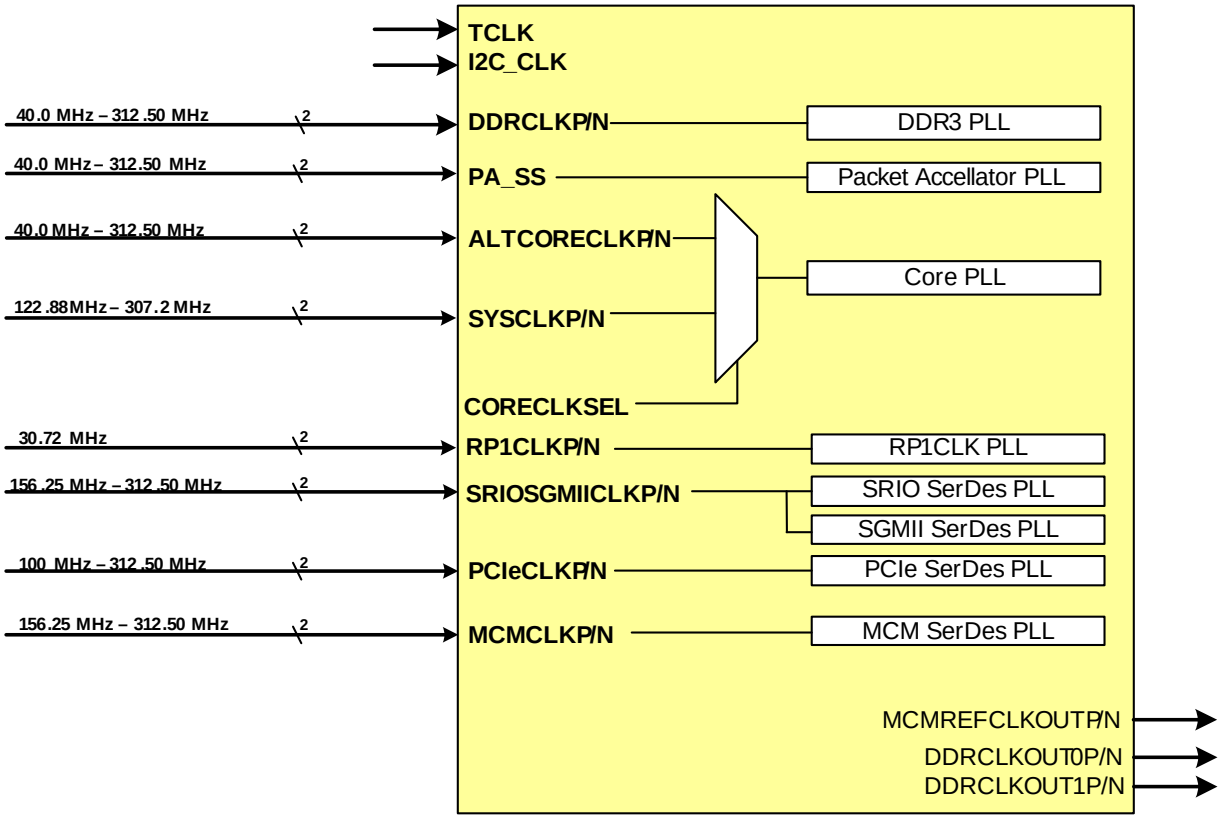
Coming out of reset, the primary device PLL will be in the PLL bypass mode.

## 3.2 PLL Reference Clock Solutions

This section describes the clock requirements and a system solution for the PLL reference clocks. There are two types of PLLs and each type has different needs for their reference clocks. The core PLL and DDR3 PLL source clocks are for digital logic, whereas the AIF, SRIO, and SGMII PLLs source clocks are for SerDes (serializer/deserializer) links.

Figure 4 illustrates how the clocks are connected to the C66x device. The frequencies listed are reference ranges only, specific requirements apply. Refer to the relative sections in this design guide for specific details on selection and implementing the clocking solution.

**Figure 4 C66x Device Reference Clocks**




The core PLL can be configured with multiplier values from ×1 to ×64 and any integer value in between as long as the PLL output frequency does not violate the maximum operating frequency for the C66x device.

There are minimum core clock frequency requirements for some peripherals so the datasheet should be referenced to check for any limitations with the desired core clock frequency. The DDR3 PLL can be configured with multiplier values from ×20 to ×33 and any integer value in between (non fractional) as long as the PLL output frequency does not violate the maximum DDR3 output operating frequency for the C66x device. Note that the PLL output is 2× the DDR3 interface clock frequency. The SerDes PLL multipliers are covered in the peripherals section.

All differential clock input buffers are low jitter clock buffers (LJCBs). These input buffers include a 100 Ω parallel termination (P to N) and common mode biasing (unless otherwise specified). Because the common mode biasing is included, the clock source must be AC coupled (except where noted in this document and data sheet). Low voltage differential swing (LVDS) and LVPECL clock sources are compatible with the LJCBs.

### 3.2.1 Unused Clock Inputs

Any unused LJCB or LVDS differential clock inputs should be connected to the appropriate rails to establish a valid logic level.

The recommended connections are shown in Figure 5. The added 1K resistor is designed to reduce power. The positive terminal should be connected to the respective power rail.

**Figure 5 Unused Clock Input Connection**

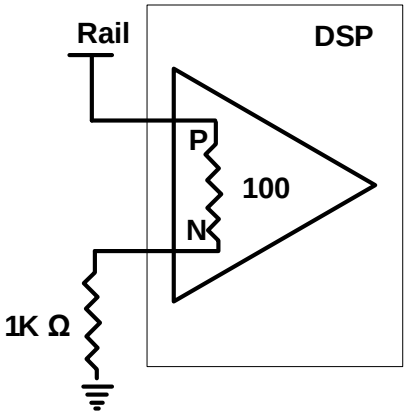



Table 3 defines the specific rails to which each unused clock input should be connected (in accordance with Figure 5).

**Table 3 Managing Unused Clock Inputs (Part 1 of 2)**

| Clock Input | Rail[1] | LJCB or LVDS |
|---|---|---|
| SYSCLKP<br>SYSCLKN | CVDD<br>GND | LJCB |
| PASSCLKP<br>PASSCLKN | CVDD<br>GND | LJCB |
| ALTCORECLKP<br>ALTCORECLKN | CVDD<br>GND | LJCB |
| SRIOSGMIICLKP<br>SRIOSGMIICLKN | CVDD<br>GND | LJCB |

**Table 3 Managing Unused Clock Inputs (Part 2 of 2)**

| Clock Input | Rail[1] | LJCB or LVDS |
|---|---|---|
| DDRCLKP<br>DDRCLKN | CVDD<br>GND | LJCB |
| PCIECLKP<br>PCIECLKN | CVDD<br>GND | LJCB |
| MCMCLKP<br>MCMCLKN | CVDD<br>GND | LJCB |
| RP1CLKP<br>RP1CLKN | DVDD1V8<br>GND | LVDS |
| RP1FBP<br>RP1FBN | DVDD1V8<br>GND | LVDS |
| **End of Table 3** | | |

1. NOTE: The power rails must be identical to those directly supporting the intended device

## 3.3 Input Clock Requirements

Table 4 defines the specific input clocking requirements for the C66x device including maximum input jitter, rise and fall times and duty cycle. Where discrepancies occur (between data sheet and this application note), always refer to the *latest* data sheet. Note that all LJCB and LVDS differential input clock buffers contain a 100 Ω internal termination resistor (no external resistor is required). Refer to Section 12 for additional information regarding SerDes configuration including tap settings in order to optimize output performance.

**Table 4 Clocking Requirements - Jitter, Duty Cycle, $T_r$ / $T_f$**

| | Logic | Input Jitter[8, 9, 10] | $T_{rise}$ / $T_{fall}$[3] | Duty Cycle % | Stability |
|---|---|---|---|---|---|
| SRIOSGMIICLKp<br>SRIOSGMIICLKn<br>(if SRIO is used) | LJCB or LVDS[1] | 4 ps RMS<br>56 ps pk-pk @ 1x10E-12 BER[7] | 50 – 350 ps[2] | 45 / 55 | ± 100 PPM |
| SRIOSGMIICLKp<br>SRIOSGMIICLKn<br>(SRIO not used) | LJCB or LVDS[1] | 8 ps RMS<br>112 ps pk-pk @ 1x10E-12 BER[7] | 50 – 350 ps[2] | 45 / 55 | ± 100 PPM |
| PCIECLKp<br>PCIECLKn | LJCB or LVDS[1] | 4 ps RMS<br>56 ps pk-pk | 50 – 350 ps[2] | 45 / 55 | ± 100 PPM |
| RPICLKp<br>RP1CLKn | LVDS | 42 ps RMS<br>600 ps pk-pk | 350 | 45 / 55 | ± 100 PPM |
| MCMCLKp<br>MCMCLKn | LJCB or LVDS[1] | 4 ps RMS<br>56 ps pk-pk @ 1x10E-15 BER[7] | 50 – 350 ps[2] | 45 / 55 | ± 100 PPM |
| ALTCORECLKp<br>ALTCORECLKn | LJCB or LVDS[1] | 100 ps pk-pk | 50 – 350 ps[2] | 45 / 55 | ± 100 PPM |
| PASSCLKp<br>PASSCLKn | LJCB or LVDS[1] | 100 ps pk-pk | 50 – 350 ps[2] | 45 / 55 | ± 100 PPM |
| SYSCLKp<br>SYSCLKn | LJCB or LVDS[1] | 4 ps RMS (56 ps pk–pk), period[5] | 50 – 350 ps[2] | 45 / 55 | ± 100 PPM |
| DDRCLKp<br>DDRCLKn | LJCB or LVDS[1] | 2.5% of DDRCLK output period (pk-pk)[4] | 50 – 350 ps[2] | 45 / 55 | ± 100 PPM |
| CORECLKp<br>CORECLKn | LJCB or LVDS[1] | 100 ps pk-pk | 50 – 350 ps[2] | 45 / 55 | ± 100 PPM |
| **End of Table 4** | | | | | |

***Notes for Table 4***

Note 1: Can be DPECL or LVPECL if properly terminated and biased.

Note 2: Swing is rated for a 250 mV (pk-pk) at zero crossing where 10% – 90% of $T_{RISE}$ and $T_{FALL}$ must occur within the prescribed 50-350 pS time frame. The minimum slew specified is relative to the minimum input signal value. An input signal must transition through:

**Minimum**

$$Vtransition = 250mV * (90\% - 10\%)$$
$$Vtransition = 250mV * 80\%$$
$$Vtransition = 200mVin \xrightarrow{in} 350\,pS$$

**and**

**Maximum**

$$Vtransition = 250mV * (90\% - 10\%)$$
$$Vtransition = 250mV * 20\%$$
$$Vtransition = 200mVin \xrightarrow{in} 50\,pS$$

Note 3: Trise/Tfall values are given for 10% to 90% of the voltage swing.

Note 4: Example 1.600 GHz (~1.25e-9 nS) * 2.5% = 32.25 pS pk-pk input jitter.

Note 5: 2 ps RMS to cover future devices in the same family, (at the release of this document the requirements are only 4 pS RMS. Specified values are when AIF2 is used, when AIF2 is not used the allowable jitter is 7.1 ps RMS or 100ps pk-pk.

Note 6: 10 kHz to 20 MHz Jitter integration bandwidth over a minimum of 10K samples.

Note 7: BER rate value specified is related to the expected output error rate based on maximum input jitter requirements listed.

Note 8: Represents total input jitter (random + deterministic) for all clock inputs.

Note 9: Final jitter numbers are based on input jitter mask values at a given frequency. The numbers provided are first approximation. Always use the jitter mask to assure input clocking requirements are met.

The two major concerns pertaining to differential reference clocks are low jitter and having the proper termination. LVDS, CML, or LVPECL clock sources can be used but they require different termination strategies. The input buffer sets its own common mode voltage so AC coupling is necessary. It also includes a 100 Ω differential termination resistor, eliminating the need for an external 100 Ω termination when using an LVDS driver. For additional information on AC termination schemes, see AC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML (SCAA059). For information on DC coupling, see DC-Coupling Between Differential LVPECL, LVDS, HSTL, and CM (SCAA062).

### 3.3.1 BER and Jitter

Excessive jitter can cause date errors, for this reason (and usually in high performance data transmission protocols) a BER (bit error rate) is usually specified to minimize the risk of an error occurring[1]. Jitter is the sum of both random and deterministic sources. In an ideal design all jitter is identified as undesirable.

Random jitter can be defined as the sum of all noise sources including components used to construct and implement the data path between source and target. Random jitter is considered unbounded and will continue to increase over time. Deterministic jitter (unlike Random Jitter) is the total jitter induced by the characteristics of the data path between source and target.

Deterministic, also referred to as “Bounded jitter” obtains its minimum or maximum phase deviation within the respective time interval. Sources of deterministic jitter include most prominently include:

- [EMI] Electromagnetic Interference radiation (from power supplies, AC power lines, & RF-signal sources).
- Crosstalk (occurs when incremental inductance from one signal line (conductor) converts an induced magnetic field from an adjacent signal line into induced current resulting in either an increase or decrease in voltage.

- Interference (Inter-Symbol Interference or ISI), increases in deterministic jitter of this nature can be caused by either "simultaneous switching" (inducing current spikes on power or ground planes possibly causing a voltage threshold level shift) or a "reflection" in the signal or transmission line (reflections result in energy flowing back through the conductor that sum with the original signal causing an amplitude variation on each conductor within a differential pair resulting in a specific time variation of the crossover (crossing) points.

Random jitter, (also referred to as "Unbounded jitter") can theoretically reach infinity. Random or unbounded jitter sources include:

- Shot noise [electron and hole noise in a semiconductor - increasing due to bias current and measurement bandwidth].
- Thermal noise [associated with electron flow in conductors, variations due to temperature, bandwidth, and noise resistance].
- Flicker or "pink" noise [spectral noise related to $1/f$].

Given a specific BER and an equivalent RMS jitter value, a peak to peak (pk-pk) jitter value can be determined (assuming a truly Gaussian or Random distribution). The following calculation can be used to approximate total jitter.

$$Jitter_{Total} = Jitter_{Random^{PK-PK}} + Jitter_{Deterministic}$$

The Random pk-pk jitter is a function of the BER and RMS jitter as denoted in the following equation:

$$Jitter_{Random^{PK-PK}} = \propto * Jitter_{RandomRMS}$$

or

$$Jitter_{RMS} = {Jitter_{pk-pk}}/{\propto}$$

| BER Rate | Number $\propto$ | BER Rate | Number $\propto$ |
|---|---|---|---|
| $10^{-4}$ | 7.438 | $10^{-11}$ | 13.412 |
| $10^{-5}$ | 8.53 | $10^{-12}$ | 14.069 |
| $10^{-6}$ | 9.507 | $10^{-13}$ | 14.698 |
| $10^{-7}$ | 10.399 | $10^{-14}$ | 15.301 |
| $10^{-8}$ | 11.224 | $10^{-15}$ | 15.883 |
| $10^{-9}$ | 11.996 | $10^{-16}$ | 16.444 |
| $10^{-10}$ | 12.723 | $10^{-17}$ | |

**Note—** $\propto$ is a calculation based on the formula: $1/2\, erfc\left(\sqrt{2*\alpha}\right) = BER$

$$Jitter_{Random^{PK-PK}} = 14.069 * 4\,pS$$ (*in this example 4pS refers to total RMS input Jitter to device*)

$$Jitter_{Random^{PK-PK}} = 56.267\,pS$$

$$Jitter_{Total} = Jitter_{Random^{PK-PK}} + Jitter_{Deterministic}$$

$$Jitter_{Total} = 56.267\,pS + 4\,pS$$ (*in this example 4pS represents the total deterministic jitter expected*)

$$Jitter_{Total} = 60.267\,pS$$

Example: SYSCLK input requirement of 4 pS (RMS jitter) and a BER rate of $10^{-15}$

$$Jitter_{Random^{PK-PK}} = 15.883 * 4\,pS$$ *(10e-15 BER * 4ps RMS Jitter)*

$$Jitter_{Random^{PK-PK}} = 63.532\,pS$$

$$Jitter_{Total} = Jitter_{Random^{PK-PK}} + Jitter_{Deterministic}$$

$$Jitter_{Total} = 63.532\,pS + 4\,pS$$

$$Jitter_{Total} = 67.532\,pS$$

Note 1: *It should be noted that a bit error rate can infer a specific limit on errors that are possible however where the error occurs and whether two errors can occur back-to-back is still possible.*

Table 5 defines the minimum and maximum input clock frequencies, termination, input clock type, and termination location for the device. Where discrepancies occur between data sheet and this application note, always refer to the *latest* data sheet. Refer to the termination section of this design guide for additional termination details. Items in **bold** represent the recommended or suggested clock input frequencies. The DDRCLKP/N input frequency will be based upon expected operating frequency (e.g., 66.667 MHz for 1333 MHz DDR3).

Additional SerDes clock requirements are identified in Section 3.5.6 that must be met and followed in order to assure a functional system. Texas Instruments has designed and evaluated specific clock sources (refer to Section 3.5) that meet and exceed the performance requirements necessary for a functional system.

**Table 5 Clocking Requirements - Input Frequency, Termination**

| | Logic | Frequency Input (MHz) Min / Typical / Max | Termination | Term. Location |
|---|---|---|---|---|
| **SRIOSGMIICLKp**<br>**SRIOSGMIICLKn**<br>(if SRIO is used) | LJCB or LVDS[1] | 156.25 / 250.00 / **312.50** | AC Couple 0.1µF | Destination Side |
| **SRIOSGMIICLKp**<br>**SRIOSGMIICLKn**<br>(SRIO not used) | LJCB or LVDS[1] | 156.25 / 250.00 / **312.50** | AC Couple 0.1µF | Destination Side |
| **PCIeCLKp**<br>**PCIeCLKn** | LJCB or LVDS[1] | 100.00 / **156.25** / 250 / 312.50 | AC Couple 0.1µF | Destination Side |
| **RPICLKp**<br>**RP1CLKn** | LVDS | **30.72** | AC Couple 0.1µF | Destination Side |
| **MCMCLKp**<br>**MCMCLKn** | LJCB or LVDS[1] | 156.25 / 250.00 / **312.50** | AC Couple 0.1µF | Destination Side |
| **ALTCORECLKp**<br>**ALTCORECLKn** | LJCB or LVDS[1] | 40.00 / **122.88** / 312.50 | AC Couple 0.1µF | Destination Side |
| **PASSCLKp**<br>**PASSCLKn** | LJCB or LVDS[1] | 40.00 / **122.88** / 312.50 | AC Couple 0.1µF | Destination Side |
| **SYSCLKp**<br>**SYSCLKn** | LJCB or LVDS[1] | 122.88 / **153.60** / 307.20 | AC Couple 0.1µF | Destination Side |
| **DDRCLKp**<br>**DDRCLKn** | LJCB or LVDS[1] | 40.00 / **66.667** / 312.50 | AC Couple 0.1µF | Destination Side |
| **CORECLKp**<br>**CORECLKn** | LJCB or LVDS[1] | 40.00 / **122.88** / 312.50 | AC Couple 0.1µF | Destination Side |
| **End of Table 5** | | | | |

1. Can be DPECL or LVPECL if properly terminated and biased.

Calculation for proper AC termination is based on the following formula:

$$C \geq 1/2 * pi * R * Freq_{MHz}$$

Where:

- R = impedance of the net (50 Ω single ended and 100 Ω differential) – each net is 50 Ω
- C = AC capacitor value derived from formula; (result are in nF)
- Freq = input frequency in Megahertz
- Pi = rounded to 3.141592654

**Note—**The pole associated with the high pass response should be placed at a minimum of two decades below the input clock frequency.

Two examples are provided, the first for an input clock of 50 MHz and the second for an input clock frequency of 312.50 MHz.

Although the results denoted in the following examples provide a minimum value, Texas Instruments recommends a minimum of 10 nF or a 0.1 µF (100 nF) ceramic capacitor be used as the AC termination value.

Example 1: **50 MHz**

$$C \geq 1/2 * pi * R_{ohms} * Freq_{MHz/100}$$

$$C \geq 1/(2 * 3.141592654 * (50) * (50e6/100))$$

$$C \geq 1/157079632.7$$

$$C \geq 6.36619nF$$

Example 2: **312.50 MHz**

$$C \geq 1/2 * pi * R_{ohms} * Freq_{MHz/100}$$

$$C \geq 1/(2 * 3.141592654 * 50 * (312.50e6/100))$$

$$C \geq 1/981747704.375$$

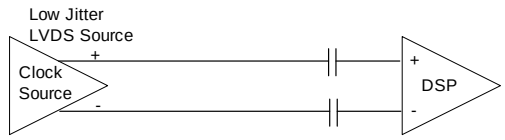
$$C \geq 1.01859e-9F$$

or 1.01859 nF

Figure 6 illustrates the typical LVDS based solution inclusive of the appropriate AC termination. AC terminations values will vary depending on many conditions but should be in the range of 0.01 µF to 1.0 µF to guarantee minimal amplitude and phase degradation of the incoming clock. Capacitor placement is critical and highly dependent upon design topology. Determination on whether the AC coupling (DC blocking) capacitors are to be staggered or in parallel and whether they are to be placed near the receiver end or elsewhere in the nets should be determined through simulation and modeling or a Signal-analysis tool typically incorporated in most common layout packages.

Ultra High Speed interfaces such as SerDes require special consideration, the parasitic capacitance of the capacitor bodies (and mounting pads) to one another and to the reference plane beneath may require a change in traditional layout techniques. Placement of the AC capacitors should also be evaluated for impact on signal integrity due to reflections.

**Figure 6 LJCB LVDS Clock Source**




For additional clocking solutions refer to the "Clocking Design Guide for KeyStone Devices" application note (SPRABI4).

## 3.4 Single Clock Source Solutions

Unlike previous Texas Instruments DSPs, the KeyStone I line of DSPs is the highest performing line of DSPs to date and does not allow for or recommend single-ended clock input sources (see Note). Differential clock inputs or clock sources provide better noise immunity and signal integrity and therefore is the clock input choice for the HPMP (High Performance MultiProcessor) DSP.

**Note—**It is possible to use a single ended clock source however the complexity and difficulty in properly biasing the circuit as well as the potential effects on signal quality, slew rates, over and under shoots make single ended solution undesirable.

## 3.5 Clocking and Clock Trees (Fan out Clock Sources)

For systems with multiple high performance device processors, it is not recommended that a single clock source be used (single output only). Excessive loading, reflections, and noise will impact performance. Instead it is recommended that differential clocking be used which include a differential clock tree.

Texas Instruments has developed a specific line of clock sources to meet the challenging requirements of today's high performance devices. In most applications the use of these specific clock sources eliminates the need for external buffers, level translators, external jitter cleaners, or multiple oscillators.

A few of the recommended parts include:

- CDCM6208* - Single PLL, 8 Differential Output Clock Tree with 4 Fractional Dividers
- CDCE62005 - Single PLL, 5 Differential Output Clock Tree with Jitter Cleaner
- CDCE62002 - Single PLL, 2 Differential Output Clock Tree with Jitter Cleaner
- CDCE62005 - Five Output Low Jitter Clock Tree with Jitter Cleaner

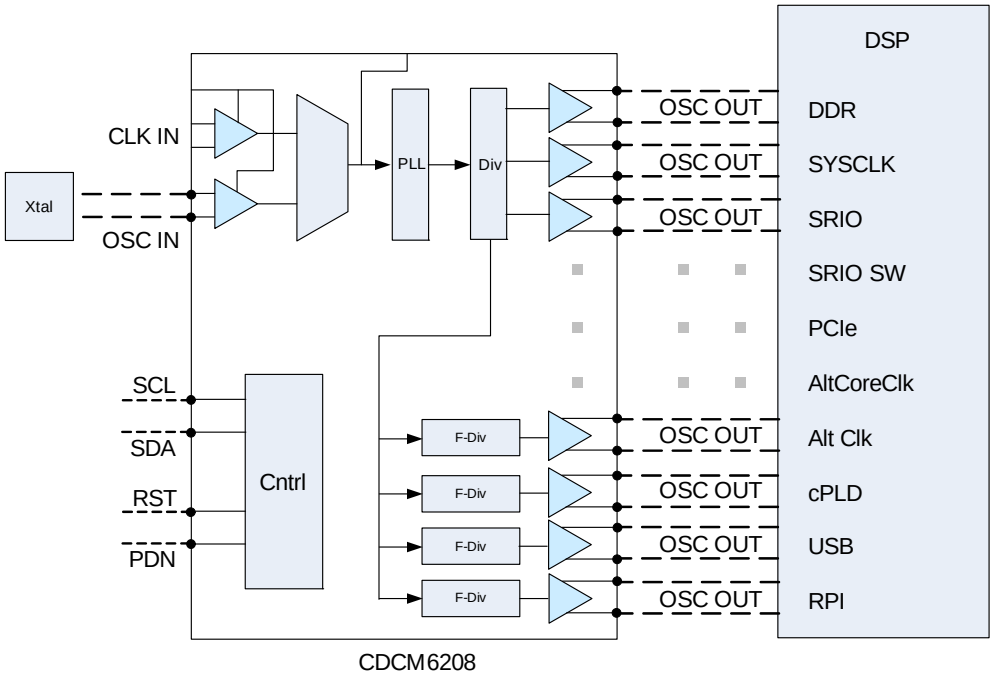
**Note—***These parts are specifically designed for the KeyStone I devices. To minimize cost and maximize performance both parts accept a differential, single-ended or crystal input clock source.

Refer to specific data sheets for clock tree input requirements and functionality.

### 3.5.1 Clock Tree Fanout Solution

The following subsection provides examples for routing between a CDCM6208/12 to one and multiple C66x devices. A similar topology should be used regardless of the end use application hardware.

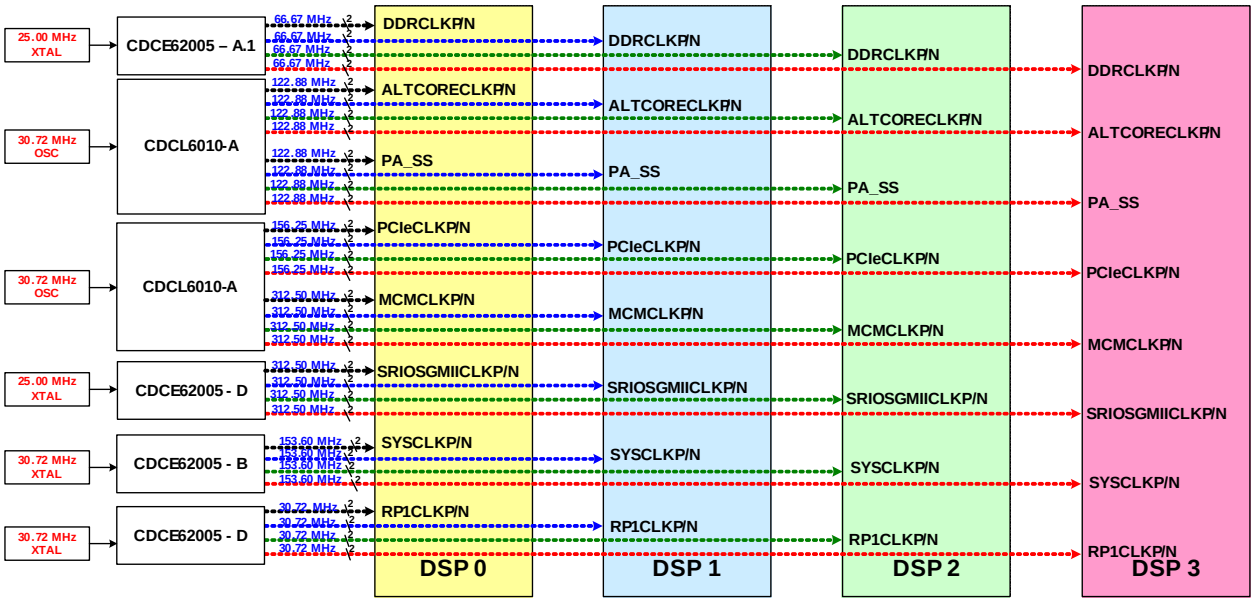
**Figure 7 Clock Fan Out - for Single Device**




The CDCM6208 incorporates fractional dividers. When assigning fractional divider outputs from the CDCM6208 it will be necessary to verify that the input jitter and performance meet or exceed the requirements for the respective device input (select the correct clock outputs for the proper clock inputs).

Figure 8 illustrates the recommended clock source as applied to multiple DSPs using alternate TI clock sources (CDCL6010 and CDCE62005). Terminations are not illustrated but must be included where required. Additional application hardware topologies may dictate different configurations based on trace lengths and routing rules, it is always recommended to model the clocking topologies to confirm that the design has been optimized.

**Figure 8 Clock Fan Out - Multiple DSPs #3**




#### 3.5.1.1 Clock Tree Layout Requirements

Key considerations when routing between clock sources and the device include the problems associated with reflections, cross talk, noise, signal integrity, signal levels, biasing, and ground references. In order to establish the optimal clocking source solution the following requirements (at a minimum) should be followed.

As with all high performance applications it is strongly recommended that you model (simulate) the clocking interface to verify the design constraints in the end use application. Application board stack up, component selection and the like all have an impact on the characteristics identified below.

Refer to the Texas Instruments *Clocking Design Guide for KeyStone Devices* application note (SPRABI4) for additional details pertaining to routing and interconnection.

### 3.5.2 Clock Tree Trace Width

Clocking trace widths are largely dependent on frequency and parasitic coupling requirements for adjacent nets on the application board. As a general rule of thumb, differential clock signals must be routed in parallel and the spacing between the differential pairs should be a minimum 2 times (2×) the trace width. Single-ended nets should have a spacing of 1.5× the distance of the widest parallel trace width.

### 3.5.3 Clock Tree Spacing

Given the variation in designs, the minimum spacing between any adjacent signals should be a minimum of 1× the width. A spacing of 1× is typically suitable for control signals (or static signals) and not data or clock nets. Single-ended or differential nets should be spaced for other nets a minimum of 1.5× and 2× respectively. A detailed cross-talk and coupling analysis (signal integrity) should be performed (modeled) before any design is released to production. An additional rule of thumb would be to maintain trace spacing ≥ three times the dielectric height (reduces ground bounce and cross talk).

### 3.5.4 Clock Transmission Lines - Microstrip versus Stripline

Refer to Section 4.3.8 for additional detail information regarding Microstrip and Stripline features and selection criteria.

### 3.5.5 Clock Component Selection & Placement

A proper clock source is critical to assure the high performance device maintains its intended functionality. TI strongly recommends the use of the clock sources developed to compliment the device (refer to Section 3.5). These clock sources have been optimized for performance, jitter, and form-factor. The recommended clock source (CDCM6208) has been designed to accept either a low frequency crystal, LVPECL, LVDS, HCSL, or LVCMOS input and are capable of sourcing either a LVPECL, LVDS, HCSL, or LVCMOS clock to the device and peripheral logic.

All clock sources should be placed as close to the targeted device(s) as possible, excessive routing induces a magnitude of problems that are costly to correct in the end product and usually require a respin of the application hardware.

Alternate clock sources have been identified and include the CDCE62002 and CDCE62005. These alternate clock sources will provide functionally identical resources when implemented correctly. Additional information regarding the CDCE62002/5 is available in the "Appendix" of this document.

### 3.5.6 Reference Clock Jitter Requirements

KeyStone I devices contain several high-performance serial interfaces commonly known as SerDes interfaces. The SerDes architecture allows for reliable data transmission without a need for common synchronized clocks. However, the architecture does require high-quality clock sources that have very little phase noise. Phase noise is also commonly referred to as clock jitter.

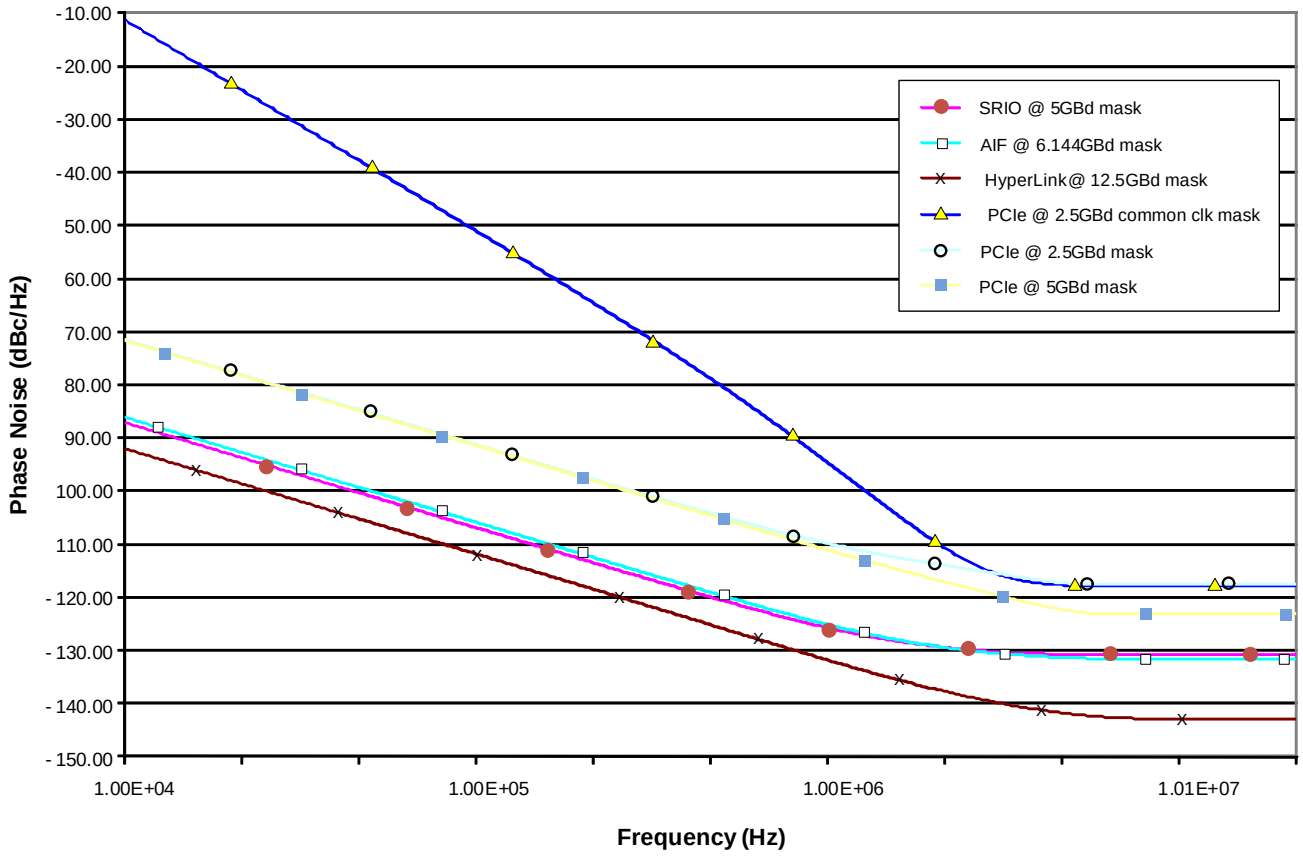
Please note that PCIe can be operated with a common clock and this allows use of spread spectrum clock sources that have higher levels of bounded phase noise. HyperLink is also defined as an interface requiring a common clock since it is expected to be a very short-reach transmission between DSPs located on the same board.

### 3.5.7 Random Jitter

Phase noise amplitude is not the only concern. The frequency content of this phase noise is also significant. Therefore, masks are provided as a means of indicating an acceptable phase noise tolerance. Each SerDes interface has a slightly different mask. SerDes data rate, input clock rate, and required bit error rate affect the phase noise tolerance.

Figure 9 shows the basic phase jitter tolerance masks for the KeyStone I SerDes interfaces. The mask shown is for the highest performance operating mode defined for each SerDes interface. Board designers must provide a reference clock that has clock jitter below the appropriate mask across the entire frequency range.

**Figure 9 SerDes Reference Clock Jitter Masks**



Since this graph may be difficult to use, we also provide this information as a straight-line approximation with the end points and the knee defined. This template is shown in Figure 10 below and the endpoints in Table 6. The mask level at specific frequencies can now be estimated based on the straight-line approximation. This is useful when comparing clock sources from various vendors who specify jitter masks in different ways.

**Figure 10 Phase Jitter Template**

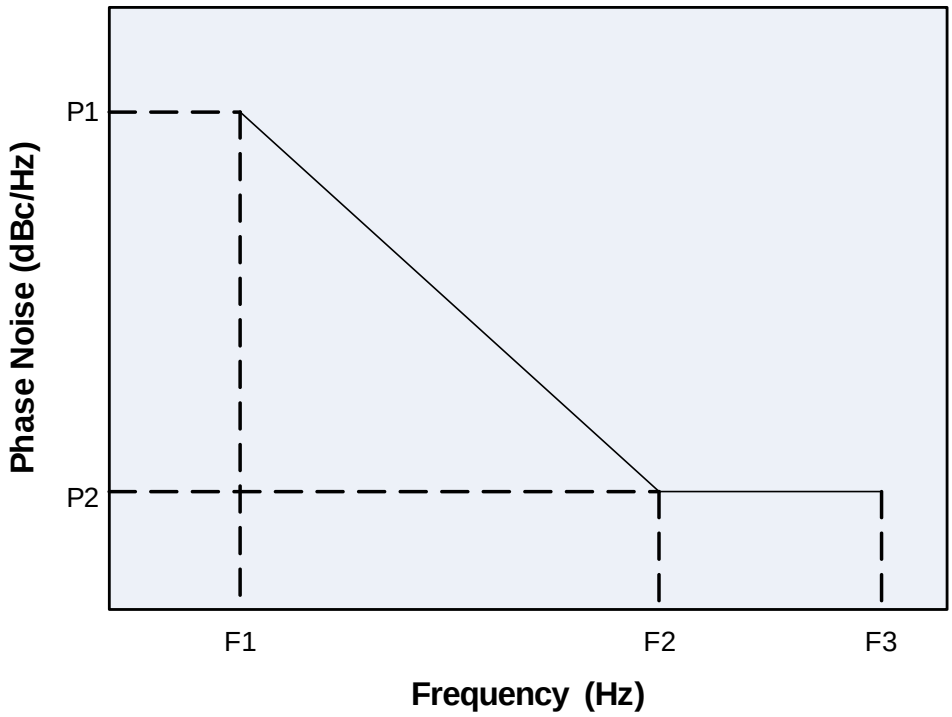



**Table 6 Phase Jitter Template Endpoints**

| Interface & Rate (GBd) | Reference Clock Frequency (MHz) | BER | F1 (kHz) | P1 (dBc/Hz) | F2 (MHz) | P2 (dBc/Hz) | F33 (MHz) |
|---|---|---|---|---|---|---|---|
| SRIO @ 5 | 250 | $1^{-15}$ | 10 | -87.1 | 1.56 | -130.8 | 20 |
| AIF @ 6.144 | 256 | $1^{-12}$ | 10 | -86.1 | 1.91 | -131.6 | 20 |
| HyperLink @ 12.5 | 250 | $1^{-17}$ | 10 | -92.1 | 3.43 | -142.9 | 20 |
| PCIe @ 2.5 | 250 (common) | $1^{-12}$ | 10 | -11.4 | 2.96 | -117.7 | 20 |
| PCIe @ 2.5 | 250 | $1^{-12}$ | 10 | -71.5 | 2.18 | -117.7 | 20 |
| PCIe @ 5 | 250 | $1^{-12}$ | 10 | -71.7 | 3.76 | -123.1 | 20 |
| **End of Table 6** | | | | | | | |

A single value also is commonly provided as the limit for phase noise. This is an integration of the phase noise across a frequency range. Table 7 shows the integrated value for each of the phase noise masks across the 10 kHz to 20 MHz frequency range and across the 1 MHz to 20 MHz frequency range. These limits are also useful for evaluating high-performance clocks sources from some vendors.

**Table 7 Phase Noise Mask Integrated Values**

| Interface & Rate (GBd) | Reference Clock Frequency (MHz) | Bit Error Rate (BER) | Rj (ps) 10kHz to 20MHz | Rj (ps) 1MHz to 20MHz |
|---|---|---|---|---|
| SRIO @ 5 | 250 | $1^{-15}$ | 4.12 | 1.17 |
| AIF @ 6.144 | 256 | $1^{-12}$ | 4.56 | 1.09 |
| HyperLink @ 12.5 | 250 | $1^{-17}$ | 2.26 | 0.33 |
| PCIe @ 2.5 | 250 (common) | $1^{-12}$ | 14030 | 8.99 |
| PCIe @ 2.5 | 250 | $1^{-12}$ | 24.59 | 5.62 |
| PCIe @ 5 | 250 | $1^{-12}$ | 23.65 | 3.37 |
| **End of Table 7** | | | | |

Please note that not all clock sources with jitter values below the single values shown in Table 7 will meet the templates shown above. These figures were generated assuming that the reference clock spectrum is shaped in the same manner as the template. Further verification may be needed.

All of the masks shown in Table 7 assume the input clock rate is about 250 MHz. The input clock rate affects the phase noise tolerance. This is because the reference clock phase noise is multiplied within the SerDes PLL. Higher levels of phase noise can be tolerated if the input reference clock rate is higher. The entire mask shifts proportional to the frequency difference. This mask offset is approximated by the equation 20*log(F2/F1). The integrated phase noise value also shifts by the same ratio. It is approximated by the equation F2/F1. Since all of the masks shown above are for 250 MHz reference clocks, the mask and phase noise adjustments from 250 MHz are shown in Table 8.

**Table 8 Mask and Phase Noise Adjustments**

| Reference Clock Frequency (MHz) | Phase Noise Mask Offset (dB) | Rj Multiplier |
|---|---|---|
| 100[1] | -8.0 | 0.40 |
| 122.88 | -6.2 | 0.49 |
| 153.60 | -4.2 | 0.61 |
| 156.25 | -4.1 | 0.63 |
| 250 | 0.0 | 1.00 |
| 312.5 | 1.9 | 1.25 |
| **End of Table 8** | | |

1. Only supported for PCIe

The phase noise masks provided are at the maximum supported data rates for SRIO, AIF, and HyperLink. Additional phase noise margin is gained when the data rate is reduced. This is because the margin for jitter increases as the data eye gets longer when the data rate decreases. Once again, the mask offset is approximated by the equation 20*log(F2/F1) and the integrated phase noise value is approximated by the equation F2/F1.

Table 9 shows the mask and phase noise adjustments for the available SRIO operating rates. Similar numbers can be computed for AIF and HyperLink. Please note that this does not apply for PCIe. The phase noise masks are defined within the PCIe specification and the masks converge at low frequency regardless of data rate as shown in Figure 10.

**Table 9 Mask and Phase Noise Adjustments**

| SerDes Data Rate (GBd) | Phase Noise Mask Offset (dB) | Rj Multiplier |
|---|---|---|
| 5 | 0.00 | 1.00 |
| 3.125 | 4.08 | 1.60 |
| 2.5 | 6.02 | 2.00 |
| 1.25 | 12.04 | 4.00 |

### 3.5.8 Deterministic Jitter

Reference clock sources may also contain deterministic jitter in the form of spurs that must also be accounted for. The effects of spurs vary depending upon whether they are correlated or uncorrelated. An exact determination of the effects of the spurs would be very complicated. (There are published papers concerning the complexities of combining the noise power of spurs.) A simplified formula is shown below.

$$Jitter_{spurs} = \frac{2}{2 \cdot pi \cdot F_{reference}} \sqrt{\sum_{1}^{N} 10^{\frac{Spurs_N\,(dBc)}{10}}} \leq 0.1ps$$

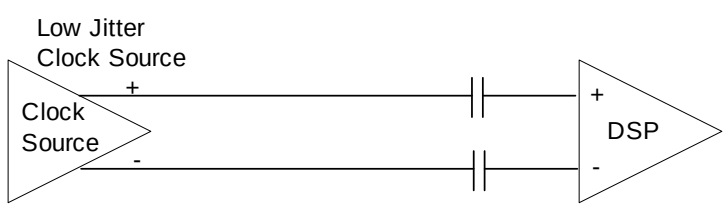
The limit of 0.1ps is a level chosen to provide a reasonable margin without complex analysis. This equation has sufficient margin to be used for all interface types and baud rates.

### 3.5.9 Clock Termination Type and Location

All input clocks are presumed to be of the differential type and require proper terminations or coupling. Each differential pair must be AC-Coupled using a 0.1 µF ceramic capacitor (0402 size or smaller recommended). In some cases, depending on topology a 1 µF capacitor can be used. All AC-Coupling capacitors should be located at the destination end as close to the device as possible.

Figure 11 denotes the intended connection between the clock source and DSP.

**Figure 11 Clock Termination Location**



### 3.5.10 Clock Signal Routing

As a general rule the following routing guidelines should be followed for all clock signals:

- All high performance clock signals should be routed on the same layer where possible; if not possible then the impact of multiple layers on performance, propagation delays and signal integrity must be taken into account.
- Clock nets, if routed internally must be captured between two planes (do not have to clock routing layers adjacent to one another).
- Clock nets involved in synchronous communications must have identical number of vias and be skew matched within 5% of the total clock period.
- Vias and terminations (if required) must be positioned in locations such that reflections do not impact signal quality or induce an unwanted change of state.
- Clock nets must be 50 Ω single ended and 100 Ω differential impedance.
- PCB impedance must be ± 5% or 47.5 Ω - 52.5 Ω for single ended clock nets.
- PCB impedance must be ± 5% or 95.0 Ω - 105 Ω for differential clock nets.
- All Microstrip clock lines must have a ground plane directly adjacent to the clock trace.
- All Stripline clock lines must have a ground or power planes directly adjacent (top & bottom) to the clock trace.
- Terminate any single ended clock signals.
- Confirm whether or not the differential clock sources require terminations.
- A ground plane must be located directly below all clock sources (oscillators, crystals).
- No digital signals must be routed underneath clock sources.
- Clock nets (source to target) must be as short as possible – emphasis on reflections.
- Complementary differential clock nets must be routed with no more then two vias, escape vias can be additional provided the escape via does not impact loading or reflections.
- Escape vias from the device or clock source must be either via-in-pad or dog-bone type design. Dog-bone designed escapes must be short enough to assure any reflections do not impact signal quality.
- The number of vias used in complementary differential clock pairs should be identical.
- Differential clock signals (complementary nets) must be skew matched to within a maximum 5 pS of one another.

## 3.6 Clock Sequencing

Table 10 defines the requirements for input clocks to the C66x device. Time frames indicated are minimum. (Refer to the part-specific data manual for specific timing requirements.)

**Note—**All clock drivers must be in a high impedance state until CVDD (at a minimum) is at a valid level. All clock inputs must either be active or in a static state with one leg pulled low and the other connected to the appropriate rail and follow the guidelines listed below and in the power sequencing section of this document.

**Table 10 Clock Sequencing**

| Clock | Condition | Sequencing |
|---|---|---|
| DDRCLK | None | Must be present 16usec before $\overline{POR}$ transitions high. |
| SYSCLK | CORECLKSEL = 0 | SYSCLK used to clock the core PLL. It must be present 16usec before $\overline{POR}$ transitions high |
| | CORECLKSEL = 1 | SYSCLK only used for AIF. Clock most be present before the reset to the AIF is removed. |
| ALTCORECLK | CORECLKSEL = 0 | ALTCORECLK is not used and should be tied to a static state |
| | CORECLKSEL = 1 | ALTCORECLK is used to clock the core PLL. It must be present 16usec before $\overline{POR}$ transitions high. |
| PASSCLK | PASSCLKSEL = 0 | PASSCLK is not used and should be tied to a static state. |
| | PASSCLKSEL = 1 | PASSCLK is used as a source for the PA_SS PLL. It must be present before the PA_SS PLL is removed from reset and programmed. |
| SRIOSGMIICLK | An SGMII port will be used | SRIOSGMIICLK must be present 16usec before $\overline{POR}$ transitions high |
| | SGMII will not be used. SRIO will be used as a boot device | SRIOSGMIICLK must be present 16usec before $\overline{POR}$ transitions high. |
| | SGMII will not be used. SRIO will be used after boot | SRIOSGMIICLK is used as a source to the SRIO SerDes PLL. It must be present before the SRIO is removed from reset and programmed. |
| | SGMII will not be used. SRIO will not be used. | SRIOSGMIICLK is not used and should be tied to a static state. |
| PCIECLK | PCIE will be used as a boot device. | PCIECLK must be present 16usec before $\overline{POR}$ transitions high. |
| | PCIE will be used after boot. | PCIECLK is used as a source to the PCIE SerDes PLL. It must be present before the PCIE is removed from reset and programmed. |
| | PCIE will not be used. | PCIECLK is not used and should be tied to a static state. |
| MCMCLK | MCM will be used as a boot device. | MCMCLK must be present 16usec before $\overline{POR}$ transitions high. |
| | MCM will be used after boot | MCMCLK is used as a source to the MCM SerDes PLL. It must be present before the MCM is removed from reset and programmed. |
| | MCM will not be used. | MCMCLK is not used and should be tied to a static state. |
| **End of Table 10** | | |

# 4 General Routing Guidelines

The following guidelines are provided as general routing rules.

## 4.1 General Routing Guidelines

- Single ended clock signals should have additional spacing to other nets to avoid cross-talk or coupling.
- Optimal performance should require trace widths to be no closer then 3× the dielectric height (between trace and adjacent ground or power plane).
- The distance between complementary differential nets must be as close as possible (typically 1× the trace width).
- Complementary differential nets must be routed in parallel for the entire length (except escapes) with identical spacing between each complementary net.
- The trace spacing between different differential pairs must be a minimum of 2 times (2×) the trace width or 2× the spacing between the complementary parasitic differential pairs.
- Do not incorporate split power/ground planes – all planes should be solid.
- Nets routed as power must be of sufficient size to accommodate the intended power plus unintended peak power requirements.
- Keep high speed signals away from the edges of the PCB. If necessary, "pin" the edges of the PCB to prevent EMI emissions.
- All signals (clocks especially) where possible should be of the differential type.
- Organize all signals into net classes prior to routing.
- All clock trace routes must be as straight as possible – minimize or eliminate serpentine routing.
- Eliminate all right angle traces. Chamfered traces (if needed) are recommended.
- Determine all constraints prior to routing respective net classes (skew, propagation delays, etc.)
- Optimize all single ended nets, minimize lengths where possible (as long as they do not violate any net class requirements or violate timing conditions).
- Place decoupling capacitors as close to the target device as possible.
- Place bulk capacitors in close proximity to their respective power supply.
- Use the largest possible vias for connecting decoupling and bulk capacitors to their respective power and ground planes – if traces to connect the decoupling capacitor to planes are used, then they must be short and wide.
- Route single-ended nets perpendicular or orthogonal to other single-ended nets to prevent coupling.
- All transmission line conductors should be as close to its respective ground plane as possible.
- All clocks should be routed on a single layer.
- Nets within a particular net class should have a matched number of vias if used (vias are not recommended if possible).
- Vias and terminations (if required) shall be positioned in locations such that reflections do not impact signal quality or induce an unwanted change of state.
- All Microstrip nets shall have a ground plane directly adjacent to the respective trace.

- All Stripline nets should have a ground or power planes directly adjacent (top & bottom) to the respective net where possible – if it is not possible to enclose the respective net within a ground/ground or ground/power stack up then at least one return path must be provided for proper operation.
- Vias and escape vias to and from the device shall be taken into account with regards to timing, reflections, loading, etc.
- It is always recommended that all net classes be modeled for optimal performance.
- Each power or ground pin should be tied to its respective plane individually.
- AC coupling capacitor as well as DC resistor termination placement shall take into account associated parasitics, coupling capacitance, and multipoint reflections. Refer to Section 4.3.8 and the Appendix for additional details.

## 4.2 SDRAM Routing Guidelines - General

There exist many different memory topologies for the C66x device. It is recommended that you follow the guidelines as identified in the DDR3 Design Guide collateral. As always, pre-layout simulations are recommended to confirm the design and functionality. Key points include:

- Maintain an acceptable level of skew across the entire DDR3 interface (by net class).
- Inductance should be $\leq$ 30 nH.
- Loading for all non-clock lines should not exceed pin loading (respective SDRAMs) plus 1.5 pF.
- Do not allow for high speed signals to cross broken or cut planes.
- Utilize proper low pass filtering on the Vref pins.
- Follow the Fly-By architecture concept for all address and control lines.
- Increase the size of the decoupling capacitor trace width as large as possible, key the stub length as short as possible.
- Add additional spacing for on clock and strobe nets to eliminate cross talk.
- Maintain a common ground reference for all bypass/decoupling capacitors, device, and SDRAMs.

### 4.2.1 SDRAM Routing Guidelines – Address Lines

The following guidelines are provided for routing the SDRAM address lines:

- All address nets should be referenced to either a solid power or ground plane (preferably the 1.5V DDR3 SDRAM power plane or Vdd).
- The entire address bus should be routed away from the data bus/nets.
- Maximum trace length for any address net should not exceed 4.5 inches (114.3 mm).
- All address nets should be skew matched to within ±0.020 inch (0.50 mm) of the device clock out to SDRAM length.
- Recommended trace to trace spacing (for address to address nets) should be no less then 0.012 inch (0.300 mm).
- The recommended trace to trace spacing (for address to other nets) should be no less then 0.020 inch (0.500 mm).
- All address and command net classes shall be skew matched to respective clock lines to within CLK ± 0.01969 inch (0.500 mm).

### 4.2.2 SDRAM Routing Guidelines – Control Lines

The following guidelines are provided for routing the SDRAM control lines:

- All control nets should be referenced to either a solid power or ground plane (preferably the DDR3 power plane is preferred).
- All control signals must be routed clear of the data signals to prevent cross coupling.
- All control group signals should be skew matched to within 0.03937 inch (1.00 mm).
- Control lines are designed to be routed from the device directly to the DRAM (point to point), fly by technology should be used in the event more than a single SDRAM is used.

### 4.2.3 SDRAM Routing Guidelines – Data Lines

The following guidelines are provided for routing the SDRAM data lines:

- The data strobe (DQS) and its complementary signal (DQS#) must be routed as a differential pair.
- All data lines must be matched length to the data strobe lines.
- Optimal layout design for DDR3 data lines would dictate that all nets be routed on the top layer and adjacent to a solid / full ground plane, and without vias.
- Any vias used (not recommended) should be modeled and taken into account with respect to timing, loading, and reflections.
- Total length from device to each SDRAM of all respective DQ and DM signals within a byte lane should be skew matched to the DQS line ± 0.03937 inch (1.00 mm).
- DQS to DQS# nets must be skew matched to ≤ 5 pS (calculate based on Tpd).

## 4.3 Specific Routing Rules and Guidelines – Net Classes

This section discusses specific design rules for the DDR3, SRIO, PCIe, HyperLink SGMII, and AIF peripherals.

### 4.3.1 DDR3 Net Classes & Specific Rules

Routing requirements for DDR3 shall follow and conform to Texas Instruments DDR3 design collateral. During implementation of the high performance DDR3 interface the following design rules should be utilized:

- All byte lanes shall be routed on the same layer. A byte lane shall include all respective address, data, DM, and DQS nets.
- All address nets shall be referenced to either a solid power or ground plane, the preferred selection would be a solid power plane.
- Address nets between the device and SDRAM (or UDIMM) should be routed away from the data and bus nets.
- All address nets should be skew matched to within ±0.020 inch (0.50 mm) of the device clock out to SDRAM length.
- The recommended trace to trace spacing (for address to address nets) should be no less than 0.012 inch (0.300 mm).
- The recommended trace to trace spacing (for address to other nets) should be no less then 0.020 inch (0.500 mm).
- All address and command net classes shall be skew matched to respective clock lines to within CLK ± 0.01969 inch (0.500 mm).

- Control signals shall be referenced to a solid plane (ground or power) – power is preferred.
- Address lines shall be routed in a "fly-by" configuration (refer to DDR3 Specification).
- Control lines shall be routed between the device and SDRAM (point to point).
- All control signals shall be routed away from data signals.
- All control group signals should be skew matched to within 0.03937 inch (1.00 mm).
- Data strobe (DQS) and the complementary signals (DQS#) shall be routed as differential pairs.
- All data lines must be matched length to the data strobe lines.
- Data lines shall be referenced to a solid ground plane. Vias are not recommended, if used, the impact of each via and the added delays induced by them shall be taken into account with respect to trace length.
- DQS to DQS# nets must be skew matched to ≤ 5 pS (calculate based on Tpd).
- Total length from device to each SDRAM of all respective DQ and DM signals within a byte lane should be skew matched to the DQS line ± 0.03937 inch (1.00 mm).
- All DDR3 input clocks shall be routed as differential pairs.
- All differential clock sources (unless otherwise specified in the data sheets) must be matched length to within 5 pS between complementary lines.
- All differential signals shall be routed in parallel with spacing between differential pairs a minimum of 1.5 times (1.5×) the trace width.
- The maximum CK/CK# to CK/CK# skew should be ≤ 5 pS.
- Differential clock signals should be routed slightly longer then the control and address lines.

There exist many different memory topologies for the C66x device. It is recommended that you follow the guidelines as identified in the DDR3 Design Guide Collateral. As always, pre-layout simulations are recommended to confirm the design and functionality. Key points include:

- Maintain acceptable levels of skew across the entire DDR3 interface (by net class).
- Inductance should be ≤ 30 nH.
- Loading for all non-clock lines should not exceed pin loading (respective SDRAMs) plus 1.5 pF.
- Do not allow for high speed signals to cross broken or cut planes.
- Utilize proper low pass filtering on the Vref pins.
- Follow the Fly-By architecture concept for all address and control lines.

### 4.3.2 SRIO Net Classes & Specific Rules

Routing requirements for the SRIO interface to the device shall adhere to good engineering practices for transmission lines operating above 6.25 GHz (actual operating frequency is 5 GHz). Specific attention shall be paid to net classes within this group and should have a high routing priority.

- Each complementary SRIO SerDes receive pair shall be individually skew matched to within 1 pS. 1 pS equates to approximately 5.464 mils to 7.092 mils (depending on propagation delays). Example of the SRIO complementary pairs include RIORXN0 & RIORXP0.

- All four complementary SRIO SerDes receive pairs shall be routed on the same layer.
- All four complementary transmit pairs shall be routed on the same layer.
- All four complementary receive pairs RIORXN/P3:0 shall be assigned and routed as an individual net class, routing skew shall not be greater than 15 pS between all receive pairs.
- All 4 complementary transmit pairs RIOTXN/P3:0 shall be assigned and routed as an individual net class, routing skew shall not be greater than 15 pS between all transmit pairs.
- Transmit and receive signals must be referenced to parallel ground planes.
- Vias are allowed and should never exceed 2 per complete net, all nets must be balanced and the impact of the via on timing and loading taken into account during design and layout.
- Differential signal routing must achieve a 100 Ω differential impedance.
- If a SRIO switch is used, the specific routing and timing requirements shall also be incorporated.

### 4.3.3 PCIe Net Classes & Specific Rules

Routing requirements for the PCIe interface shall adhere to good engineering practices for transmission lines operating above 5 GHz. Specific attention shall be paid to net classes within this group and should have a high routing priority (if this interface is used).

- Each complementary PCIe SerDes receive pair shall be individually skew matched to within 1 pS. 1 pS equates to approximately 5.464 mils to 7.092 mils (depending on propagation delays). Example of complementary pairs include PCIERXN0 & PCIERXP0.
- Both complementary PCIe SerDes receive pairs shall be routed on the same layer.
- Both complementary PCIe SerDes transmit pairs shall be routed on the same layer.
- Both complementary PCIe receive pairs PCIERXN/P1:0 shall be assigned to an individual net class where routing skew shall not be greater than 5 pS between all receive pairs.
- All complementary PCIe transmit pairs PCIETXN/P1:0 shall be assigned to an individual net class and routing skew shall not be greater than 10 pS between all transmit pairs.
- Transmit and receive signals must be referenced to parallel ground planes.
- Vias are allowed and should never exceed 2 per net, all nets must be balanced and the impact of the via on timing, reflections, and loading taken into account during design and layout. This interface should be modeled to assure functionality.
- Differential signal routing must achieve a 100 Ω differential impedance.

**Note—**Vias in PCIe nets are typically not recommended and pose problems if not implemented correctly with regard to signal integrity.

### 4.3.4 HyperLink Net Classes & Specific Rules

- Each differential receive pair shall be individually skew matched to within 1 pS (absolute maximum). 1 pS equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). An example of a differential pair is MCMRXN0 & MCMRXP0.
- All differential receive pairs shall be routed on the same layer.
- Each differential transmit pair shall be individually skew matched to within 1 pS (absolute maximum). 1 pS equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). An example of a differential pair is MCMTXN0 & MCMTXP0.
- All differential transmit pairs shall be routed on the same layer.
- All differential receive pairs MCMRXN/P3:0 shall be assigned to an individual net class and routing skew shall not be greater than 100 pS (absolute maximum) between all receive pairs.
- All differential transmit pairs MCMTXN/P3:0 shall be assigned to an individual net class and routing skew shall not be greater than 100 pS (absolute maximum) between all transmit pairs.
- All differential pairs shall be < 4.0” (101.6 mm) in total length, recommended length is 2.00” (50.8 mm).
- The MCMRXFLCLK & MCMRXFLDAT nets shall be skew matched within 250 pS (absolute maximum) of one another.
- The MCMTXFLCLK & MCMTXFLDAT nets shall be skew matched within 250 pS (absolute maximum) of one another.
- The MCMRXPMCLK & MCMRXPMDAT nets shall be skew matched within 250 pS (absolute maximum) of one another.
- The MCMTXPMCLK & MCMTXPMDAT nets shall be skew matched within 250 pS (absolute maximum) of one another.
- Transmit and receive signals must be referenced to continuous, parallel ground planes.
- Differential signal routing must achieve 100-ohm differential impedance.
- Routing shall take into account propagation delays between microstrip and strip line topologies.
- To prevent crosstalk ina simple board stack-up, we recommend that the differential receive pairs be routed as microstrip (outer layer) on one side of the board and the differential transmit pairs be routed as microstrip (outer layer) on the other side of the board.
- Up to 2 vias are allowed but there must be no stub and the differential nature of the circuit must be maintained. This forces routing on the outer layers unless blind via technologies or back-drilling are used.
- If a via is implemented, an adjacent ground via will be implemented to minimize the discontinuity.
- HyperLink lanes can be swapped to simplify routing. The differential pairing must be maintained.
- P and N connections for a single differential pair can be inverted to simplify routing.
- The HyperLink interface is intended for DC coupled operation between two DSPs on a single board.

Board layout simulation is a requirement for this class of circuit to validate the PCB routing.

### 4.3.5 SGMII Net Classes & Specific Rules

Routing requirements for the SGMII or Ethernet interface must adhere to good engineering practices for transmission lines operating at or above 1 GHz. Specific attention must be paid to net classes within this group and should have a high routing priority. The device incorporates SerDes outputs and requires the use of a PHY to interconnect to a standard RJ-45 connector.

- Each complementary device SerDes receive pair must be individually skew matched to within 5 pS. 5 pS equates to approximately 27.32 mils to 35.46 mils (depending on propagation delays). Example of complementary pairs include SGMIIRXN0 & SGMIIRXP0.
- Both complementary device SerDes receive pairs must be routed on the same layer.
- Each complementary device SerDes transmit pairs must be skew matched to within 5 pS. 5 pS equates to approximately 27.32 mils to 35.46 mils (depending on propagation delays). Example of complementary SerDes pairs include: SGMIITXN0 & SGMIITXP0.
- All complementary device transmit pairs must be routed on the same layer.
- All complementary device receive pairs (SGMIIRXN/P3:0) must be assigned to an individual net class and routing skew must not be greater then 10 pS between all receive pairs.
- All complementary device transmit pairs (SGMIITXN/P3:0) must be assigned to an individual net class and routing skew must not be greater then 10 pS between all transmit pairs.
- Transmit and receive signals must be referenced to parallel ground planes.
- Vias are allowed and should never exceed two per net, all nets must be balanced and the impact of the via on timing and loading taken into account during design and layout.
- All net signals must be referenced to a parallel ground plane.
- Differential signal routing must achieve a 100 Ω differential impedance.

### 4.3.6 AIF Net Classes & Specific Rules

Routing requirements for the AIF (RP3) interface must adhere to good engineering practices for transmission lines operating at or above 1 GHz. Specific attention must be paid to net classes within this group and should have a high routing priority. The device incorporates SerDes outputs which typically connect directly to the antenna interface (through a back plane) or between devices (for serial and parallel processing).

- Each complementary device SerDes receive pair must be individually skew matched to within 5 pS. 5 pS equates to approximately 27.32 mils to 35.46 mils (depending on propagation delays). Example of complementary pairs include AIFRXN0 & AIFRXP0.
- Both complementary device SerDes receive pairs must be routed on the same layer.
- Each complementary device SerDes transmit pairs must be skew matched to within 5 pS. 5 pS equates to approximately 27.32 mils to 35.46 mils (depending on propagation delays). Example of complementary SerDes pairs include: AIFTXN0 & AIFTXP0.

- All complementary device transmit pairs must be routed on the same layer.
- All complementary device receive pairs (AIFRXN/P5:0) must be assigned to an individual net class and routing skew must not be greater than 10 pS between all receive pairs.
- All complementary device transmit pairs (AIFTXN/P5:0) must be assigned to an individual net class and routing skew must not be greater than 10 pS between all transmit pairs.
- Transmit and receive signals must be referenced to parallel ground planes.
- Vias are allowed and should never exceed two per net, all nets must be balanced and the impact of the via on timing and loading taken into account during design and layout.
- All net signals must be referenced to a parallel ground plane.
- Differential signal routing must achieve a 100 Ω differential impedance.

### 4.3.7 General Trace Width Requirements

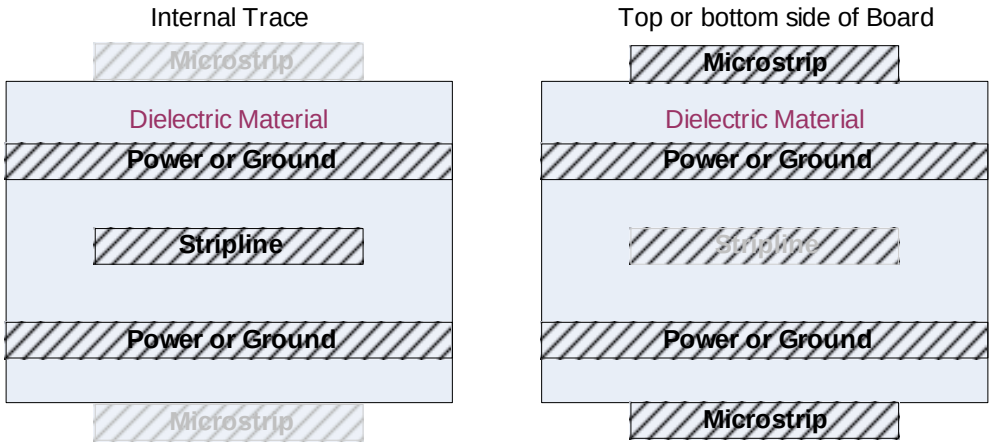
Trace widths are largely dependent on frequency and parasitic coupling requirements for adjacent nets within the application design. As a general rule of thumb, and given the complexity of many markets utilizing these high performance devices, a typical trace width is on the order of 4 mils or 0.1016 mm. Trace widths of this size typically allow for better routing and improved routing densities.

Spacing to other traces is a function of the stack up impedance as well as induced isolation to minimize (eliminate) cross talk. Most single ended nets have a width of 4 mils (0.1016 mm) and are spaced a minimum of 1.5× the trace width from all other traces (2× the trace width is recommended).

### 4.3.8 Clock & High Performance Transmission Lines - Microstrip versus Stripline

Clock nets (and most other high performance nets) are typically designed for either a microstrip or stripline topology. Figure 12 illustrates the difference between a microstrip and a stripline topology.

**Figure 12 Stripline and Microstrip Topologies**



The most obvious difference between these two topologies is the location of the respective net (trace). In a stripline topology (left side) the net or trace is embedded in the PCB and usually between ground or power layers. In the Microstrip topology (right side) the net or trace is on an outer layer and adjacent to a power or ground plane.

There exist several reasons why one (Stripline versus Microstrip) topology would be selected over the other, key factors determining which topology is used includes:

- **Interconnection** - The number of pins on the interconnecting devices may limit the section.
- **Performance** - High speed signals should not be routed on multiple layers, generally on the top layers.
- **EMI** - Where emissions or the susceptibility to spurious radiation may impact signal integrity, stripline topologies are recommended.
- **Timing** - Propagation delays differ between Microstrip and stripline topologies, the use of either must be comprehended for any / all timing critical nets.
- **Routing** - The routing of high speed clock signals is critical to a functional design; proper return current paths to minimize switching noise is essential. Routing clocks that are > 250 MHz should be done using a Microstrip topology as long as they are <2 inches (50.8 mm) in length.

In order to determine the timing effects (Tpd) between a Microstrip and Stripline topology the following equations are provided (pS/in). A third equation is provided as a method for calculating values in mm/nS (microstrip).

**Equation 1: Microstrip Equation (pS/in)**

$$T_{PD}\ (Microstrip) = 85 * \sqrt{(0.475\,\varepsilon r + 0.67)}$$

**Equation 2: Stripline Equation (pS/in)**

$$T_{PD}(Stripline) = 85 * \sqrt{\varepsilon r}$$

**Equation 3: Propagation Delay Calculation (alternative) (mm/pS)**

$$T_{PD} = \frac{l}{V_P} \rightarrow where \rightarrow \left( V_p = \frac{C}{\sqrt{Er}} \right) \rightarrow where \rightarrow \text{ C = 300 mm per nS or 0.300 m/pS}$$

To determine the impact on timing (propagation delay) the following example is provided:

***Given*** Er = 4.5; trace length = 2” (50.8 mm)

**Example**

$$T_{PD}\,(Microstrip) = 85 * \sqrt{(0.475\,\varepsilon r + 0.67)}$$

$$T_{PD}(Microstrip) = 85 * \sqrt{(0.475 * 4.5 + 0.67}$$

$$T_{PD}(Microstrip) = 85 * \sqrt{(2.1375 + 0.67}$$

$$T_{PD}(Microstrip) = 85 * \sqrt{2.8075}$$

$$T_{PD}(Microstrip) = 85 * 1.676$$

$$T_{PD}(Microstrip) = 142.42\,ps/in$$

$$T_{PD}(2''\,Microstrip) = 284.84\,ps$$

$$T_{PD}(Stripline) = 85 * \sqrt{\varepsilon r}$$

$$T_{PD}(Stripline) = 85 * \sqrt{4.5}$$

$$T_{PD}(Stripline) = 85 * 2.12132$$

$$T_{PD}(Stripline) = 180.31\,ps/in$$

$$T_{PD}(2''\,Stripline) = 360.62\,ps$$

**Example**

$$T_{PD} = l/V_P \rightarrow where \rightarrow \left(V_p = \frac{C}{\sqrt{Er}}\right)$$

$$T_{PD} = l/V_P \rightarrow where \rightarrow \left(V_p = \frac{0.300}{\sqrt{4.5}}\right)$$

$$T_{PD} = l/V_P \rightarrow where \rightarrow \left(V_p = 0.141421356\right)$$

$$T_{PD} = 50.8/0.141421356 \rightarrow 359.21\,pS$$

**Summary** The difference between the two topologies is calculated at 37.89 pS/in (with FR4 material with an Er of 4.5) where the Microstrip has a faster propagation time.

**Note** Calculations can also be performed for longer Microstrip and Stripline topologies in nS/ft rather than pS/in using the following formulas respectively:

$$T_{PD}(Microstrip_{nS/ft}) = 1.017 * \sqrt{(0.475\varepsilon r + 0.67}$$

Or

$$T_{PD}(Stripline_{nS/ft}) = 1.017 * \sqrt{\varepsilon r}$$

Table 11 and Table 12 provide simple approximations between trace length in inches and millimeters to propagation delays in pS (picoseconds).

**Table 11 Trace Propagation Delays - Trace Length in Inches Versus Delay in pS**

| Common Name | | | Trace Length in Inches Versus Delay in pS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Er** | | **µ Strip** | **1″** | **2″** | **3″** | **4″** | **5″** | **6″** | **7″** | **8″** | **9″** | **10″** |
| 1 | Air | 90.9540 | 90.95 | 181.91 | 272.86 | 363.82 | 454.77 | 545.72 | 636.68 | 727.63 | 818.59 | 909.54 |
| 2.2 | PTFE/Glass | 111.3143 | 111.31 | 222.63 | 333.94 | 445.26 | 556.57 | 667.89 | 779.20 | 890.51 | 1001.83 | 1113.14 |
| 2.9 | Ceramic | 121.6273 | 121.63 | 243.25 | 364.88 | 486.51 | 608.14 | 729.76 | 851.39 | 973.02 | 1094.65 | 1216.27 |
| 3.5 | GETEK | 129.8165 | 129.82 | 259.63 | 389.45 | 519.27 | 649.08 | 778.90 | 908.72 | 1038.53 | 1168.35 | 1298.17 |
| 4 | FR-4 | 136.2654 | 136.27 | 272.53 | 408.80 | 545.06 | 681.33 | 817.59 | 953.86 | 1090.12 | 1226.39 | 1362.65 |
| 4.1 | FR-4 | 137.5189 | 137.52 | 275.04 | 412.56 | 550.08 | 687.59 | 825.11 | 962.63 | 1100.15 | 1237.67 | 1375.19 |
| 4.2 | FR-4 | 138.761 | 138.76 | 277.52 | 416.28 | 555.04 | 693.81 | 832.57 | 971.33 | 1110.09 | 1248.85 | 1387.61 |
| 4.3 | FR-4 | 139.9922 | 139.99 | 279.98 | 419.98 | 559.97 | 699.96 | 839.95 | 979.95 | 1119.94 | 1259.93 | 1399.92 |
| 4.4 | FR-4 | 141.2126 | 141.21 | 282.43 | 423.64 | 564.85 | 706.06 | 847.28 | 988.49 | 1129.70 | 1270.91 | 1412.13 |
| 4.5 | FR-4 | 142.4226 | 142.42 | 284.85 | 427.27 | 569.69 | 712.11 | 854.54 | 996.96 | 1139.38 | 1281.80 | 1424.23 |
| **Er** | | **Stripline** | **1″** | **2″** | **3″** | **4″** | **5″** | **6″** | **7″** | **8″** | **9″** | **10″** |
| 1 | Air | 58.5822 | 58.58 | 117.16 | 175.75 | 234.33 | 292.91 | 351.49 | 410.08 | 468.66 | 527.24 | 585.82 |
| 2.2 | PTFE/Glass | 86.8915 | 86.89 | 173.78 | 260.67 | 347.57 | 434.46 | 521.35 | 608.24 | 695.13 | 782.02 | 868.92 |
| 2.9 | Ceramic | 99.7619 | 99.76 | 199.52 | 299.29 | 399.05 | 498.81 | 598.57 | 698.33 | 798.10 | 897.86 | 997.62 |
| 3.5 | GETEK | 109.5973 | 109.60 | 219.19 | 328.79 | 438.39 | 547.99 | 657.58 | 767.18 | 876.78 | 986.38 | 1095.97 |
| 4 | FR-4 | 170.000 | 170.00 | 340.00 | 510.00 | 680.00 | 850.00 | 1020.00 | 1190.00 | 1360.00 | 1530.00 | 1700.00 |
| 4.1 | FR-4 | 172.1119 | 172.11 | 344.22 | 516.34 | 688.45 | 860.56 | 1032.67 | 1204.78 | 1376.90 | 1549.01 | 1721.12 |
| 4.2 | FR-4 | 174.1982 | 174.20 | 348.40 | 522.59 | 696.79 | 870.99 | 1045.19 | 1219.39 | 1393.59 | 1567.78 | 1741.98 |
| 4.3 | FR-4 | 176.2598 | 176.26 | 352.52 | 528.78 | 705.04 | 881.30 | 1057.56 | 1233.82 | 1410.08 | 1586.34 | 1762.60 |
| 4.4 | FR-4 | 178.2975 | 178.30 | 356.60 | 534.89 | 713.19 | 891.49 | 1069.79 | 1248.08 | 1426.38 | 1604.68 | 1782.98 |
| 4.5 | FR-4 | 180.3122 | 180.31 | 360.62 | 540.94 | 721.25 | 901.56 | 1081.87 | 1262.19 | 1442.50 | 1622.81 | 1803.12 |
| **End of Table 11** | | | | | | | | | | | | |

**Table 12 Trace Propagation Delays - Trace Length in Millimeters Versus Delay in pS (Part 1 of 2)**

| | Common Name | µ Strip | Trace Length in Millimeters Versus Delay in pS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Er** | | **1** | **10** | **20** | **30** | **40** | **50** | **60** | **70** | **80** | **90** | **100** |
| 1 | Air | 3.5809 | 35.81 | 71.62 | 107.43 | 143.23 | 179.04 | 214.85 | 250.66 | 286.47 | 322.28 | 358.09 |
| 2.2 | PTFE/Glass | 4.3825 | 43.82 | 87.65 | 131.47 | 175.30 | 219.12 | 262.95 | 306.77 | 350.60 | 394.42 | 438.25 |
| 2.9 | Ceramic | 4.7885 | 47.88 | 95.77 | 143.65 | 191.54 | 239.42 | 287.31 | 335.19 | 383.08 | 430.96 | 478.85 |
| 3.5 | GETEK | 5.1109 | 51.11 | 102.22 | 153.33 | 204.44 | 255.54 | 306.65 | 357.76 | 408.87 | 459.98 | 511.09 |
| 4 | FR-4 | 5.3648 | 53.65 | 107.30 | 160.94 | 214.59 | 268.24 | 321.89 | 375.53 | 429.18 | 482.83 | 536.48 |
| 4.1 | FR-4 | 5.4141 | 54.14 | 108.28 | 162.42 | 216.57 | 270.71 | 324.85 | 378.99 | 433.13 | 487.27 | 541.41 |
| 4.2 | FR-4 | 5.4630 | 54.63 | 109.26 | 163.89 | 218.52 | 273.15 | 327.78 | 382.41 | 437.04 | 491.67 | 546.30 |
| 4.3 | FR-4 | 5.5115 | 55.12 | 110.23 | 165.35 | 220.46 | 275.58 | 330.69 | 385.81 | 440.92 | 496.04 | 551.15 |
| 4.4 | FR-4 | 5.5596 | 55.60 | 111.19 | 166.79 | 222.38 | 277.98 | 333.57 | 389.17 | 444.76 | 500.36 | 555.96 |
| 4.5 | FR-4 | 5.6072 | 56.07 | 112.14 | 168.22 | 224.29 | 280.36 | 336.43 | 392.50 | 448.58 | 504.65 | 560.72 |

**Table 12 Trace Propagation Delays - Trace Length in Millimeters Versus Delay in pS (Part 2 of 2)**

| | Common Name | Stripline | Trace Length in Millimeters Versus Delay in pS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Er** | | **1** | **10** | **20** | **30** | **40** | **50** | **60** | **70** | **80** | **90** | **100** |
| 1 | Air | 2.3064 | 2.31 | 23.06 | 46.13 | 69.19 | 92.26 | 115.32 | 138.38 | 161.45 | 184.51 | 207.57 |
| 2.2 | PTFE/Glass | 3.4209 | 3.42 | 34.21 | 68.42 | 102.63 | 136.84 | 171.05 | 205.26 | 239.46 | 273.67 | 307.88 |
| 2.9 | Ceramic | 3.9276 | 3.93 | 39.28 | 78.55 | 117.83 | 157.11 | 196.38 | 235.66 | 274.93 | 314.21 | 353.49 |
| 3.5 | GETEK | 4.3149 | 4.31 | 43.15 | 86.30 | 129.45 | 172.59 | 215.74 | 258.89 | 302.04 | 345.19 | 388.34 |
| 4 | FR-4 | 6.6929 | 6.69 | 66.93 | 133.86 | 200.79 | 267.72 | 334.65 | 401.57 | 468.50 | 535.43 | 602.36 |
| 4.1 | FR-4 | 6.7761 | 6.78 | 67.76 | 135.52 | 203.28 | 271.04 | 338.80 | 406.56 | 474.32 | 542.08 | 609.85 |
| 4.2 | FR-4 | 6.8582 | 6.86 | 68.58 | 137.16 | 205.75 | 274.33 | 342.91 | 411.49 | 480.07 | 548.66 | 617.24 |
| 4.3 | FR-4 | 6.9394 | 6.94 | 69.39 | 138.79 | 208.18 | 277.57 | 346.97 | 416.36 | 485.76 | 555.15 | 624.54 |
| 4.4 | FR-4 | 7.0196 | 7.02 | 70.20 | 140.39 | 210.59 | 280.78 | 350.98 | 421.18 | 491.37 | 561.57 | 631.76 |
| 4.5 | FR-4 | 7.0989 | 7.10 | 70.99 | 141.98 | 212.97 | 283.96 | 354.95 | 425.93 | 496.92 | 567.91 | 638.90 |
| **End of Table 12** | | | | | | | | | | | | |

## 4.4 PCB Material Selection

Proper pcb (printed circuit board) material [also referred to as pwb (printed wiring board) has a large impact on the impedance of the stack up and even more impact on the propagation delays of signals.

Table 11 also illustrates the approximate dielectric constant (Er) differences for common pwb materials used today. Selection of material is paramount to a successful design. Special consideration must be taken if routing signals on different layers where timing is concerned (except where not allowed by this design guide).

## 4.5 PCB Copper Weight

Proper copper thickness (referred to as planes) is important to the overall impedance, thermal management, and current carrying capabilities of the design. During the examination and review of all application hardware it is important to consider each of these variables.

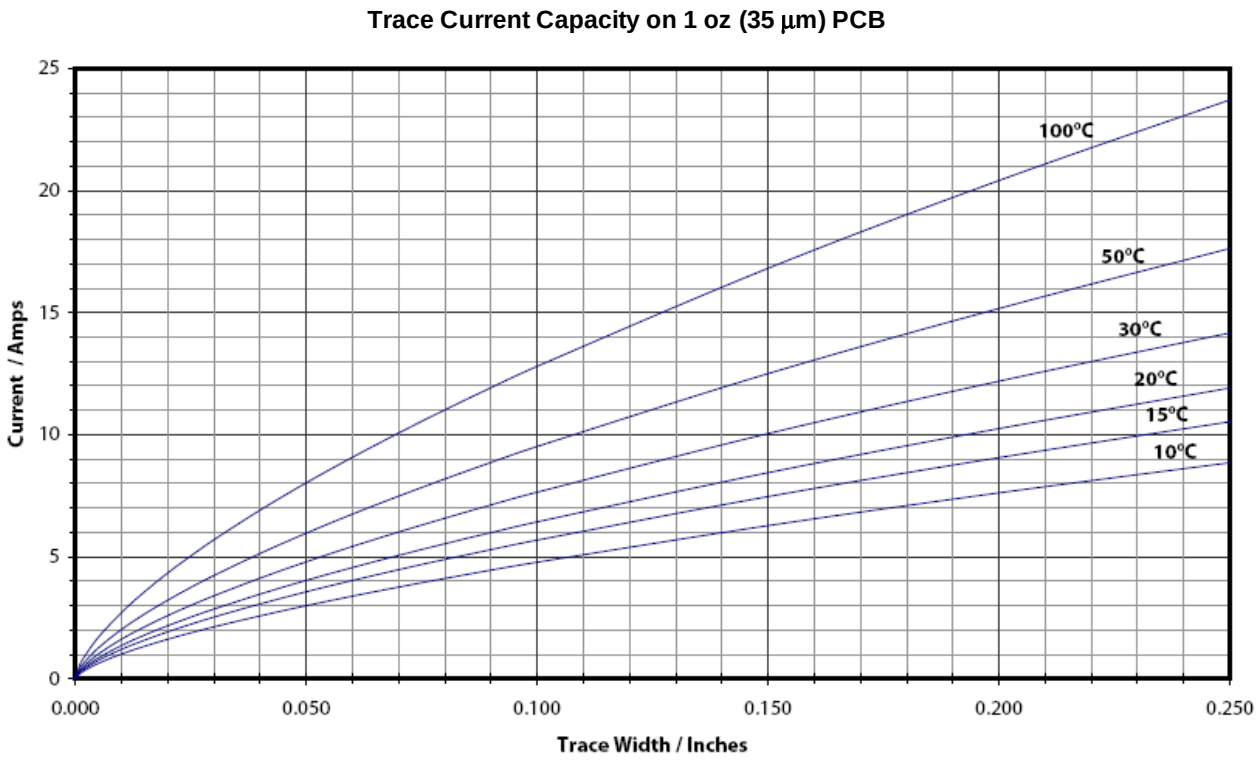
As a general rule of thumb, the inner layers or planes of most PCBs are typically 1 oz copper while the outer layers are 0.5 oz copper. Outer layers receive solder masking which in the finished product is usually similar to the 1 oz inner copper weight. Table 13 provides basic information regarding copper weight, thickness and current carrying capabilities (other factors can positively or negatively affect these specifications).

**Table 13 Copper Weight and Thickness**

| Cu Weight | Cu Thickness (mils) | Cu Thickness (mm) |
|---|---|---|
| 2.0 oz | 2.8 | 0.07112 |
| 1.0 oz | 1.4 | 0.03556 |
| ½ oz | 0.7 | 0.01778 |

Figure 13 illustrates the relationship between trace width, copper thickness (1 oz. shown) and current carrying capability.

**Figure 13 Trace Width to Current Specifications**



# 5 Power Supplies

The C66x device supply rails should be generated using the recommended power supplies. The following section defines the minimum requirements for all C66x device power supply rails.

## 5.1 Power Planes

The following section defines the recommended power planes for the C66x device as well as the implementation details and requirements. Figure 14 illustrates the minimum set of power planes the device includes. Refer to the specific data sheet for additional power planes.

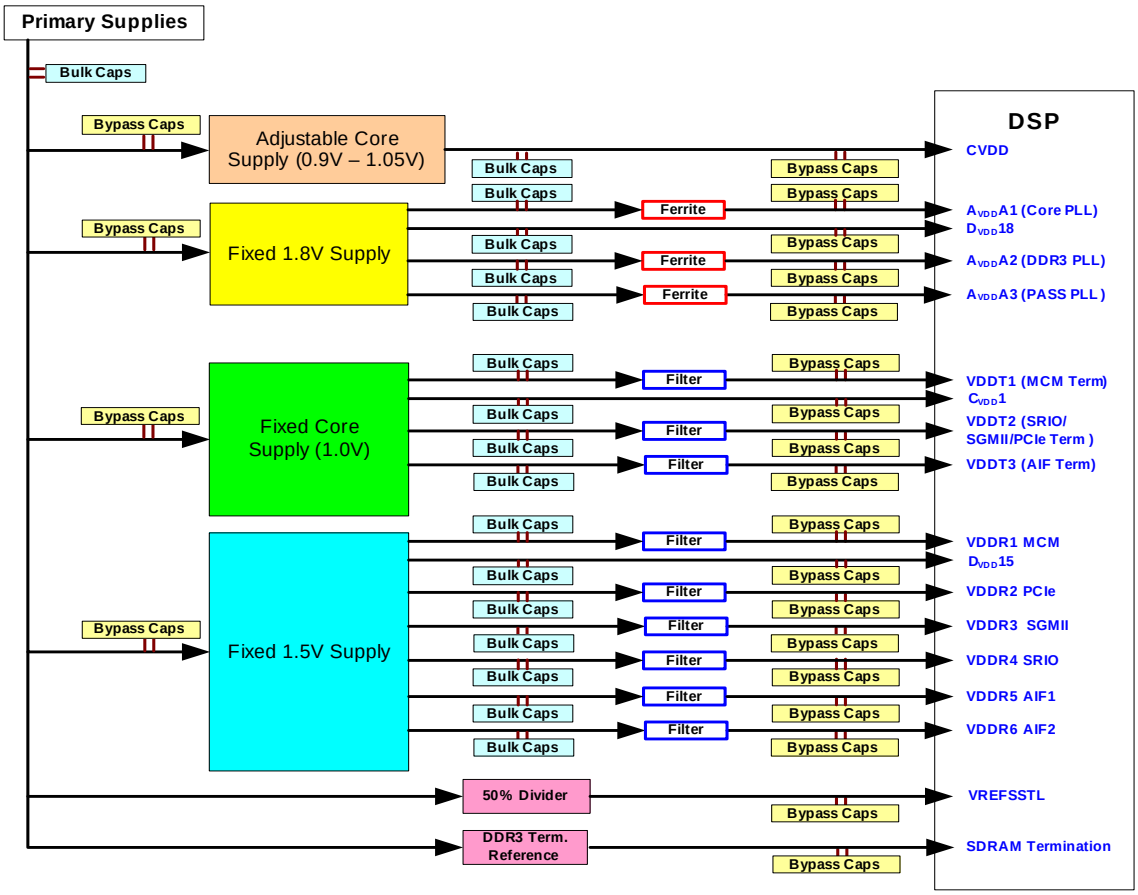
Power supply requirements are highly dependent on the use case selected. This includes which peripherals are used as well as the operating frequencies where applicable for each peripheral. For additional detailed information, refer to the *KeyStone Power Consumption Summary* application report (SPRABF2). All recommended power supplies and margins are based on initial silicon power estimates and initial power measurements.

Depending on the design and usage, the worse-case transient conditions should always be taken into account when designing and evaluating power supplies and associated capacitors.

Designs outside of those recommended in this application note should not be used. All conditions and use cases beyond those identified in this application note and the *KeyStone Power Consumption Summary* application report are note recommended and should not be used to estimate thermal performance.

Each power plane is required even if the peripheral associated with the supply is not used (unless specified).

**Figure 14 DSP Power Supply Planes (Rails)**




### 5.1.1 Voltage Plane IR Drop

All device supply rail voltage gradients (IR drops) need to be considered. All devices located in close proximity to the referenced power supply will have a slightly higher voltage than devices situated farther from the respective power supply which will have a slightly lower voltage. This voltage differential can be minimized by making the copper planes thicker or by spacing the devices across a wider area of the plane. Be sure to consider both the core power plane(s) and the ground plane(s).

The resistance of the plane can be determined by the following formula:

R = rho * length/(width * thickness)

where rho is the resistivity of copper equal to 1.72E-8 Ω-meters. PCB layer thickness is normally stated in *ounces*. One ounce of copper is about 0.012 inches or 30.5E-6 meters thick. The width must be de-rated to account for vias and other obstructions. A 50 mm wide strip of 1 oz copper plane derated 50% for vias has a resistance of 0.57 mΩ per inch (14.478 mΩ per mm).

## 5.2 Device Power Rails

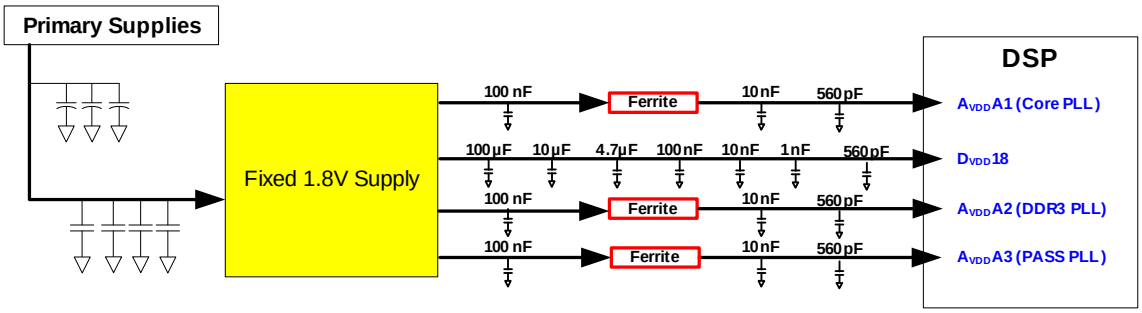
The C66x device has at a minimum four separate power supply rails. Each rail has specific requirements regarding current, ripple, and tolerance that must be strictly enforced. The following table defines the common device power rails and supply requirements.

## 5.3 Power Supply Filters

The following section defines the recommended power plane filters for the C66x device as well as the implementation details and requirements.

Filters are recommended for most all KeyStone I device voltage rails. An overview of the recommended power supply generation architecture is shown in Figure 15 (1.8 V supply rail only shown).

**Figure 15 Power Supply Filter (example)**




### 5.3.1 Filters versus Ferrite Beads

In past devices, EMI filters (commonly referred to as "T-filters") have been utilized to condition power rails which may be susceptible to induced noise. These filters acted as low-pass, band-pass, or high-pass filters (depending on selection) limiting parasitic coupled noise on each respective power plane/supply. These EMI filters solve many problems typically overlooked by designers which may result in device related problems on production boards.

Ferrite beads also were evaluated based on performance, physical form factor, and cost. Ferrites did offer a lower cost point and benefit and therefore are required (by TI) for the PLL supplies. Refer to Table 14 for recommended ferrite filters. Key to selecting the EMI filter and ferrites are cut off frequency and current rating.

Table 14 defines the characteristics necessary for selecting the proper T-filter. The following specifications must be adhered to for proper functionality. Refer to the power supply bulk and decoupling capacitor section for additional details necessary to design an acceptable power supply system.

**Table 14 Power Rail Filter Recommendations (Part 1 of 2)**

| Power Rail | Voltage | Filter (p/n) | Mfg | Current | Insertion Loss (dB)/ Impedance | Capacitance/DCR |
|---|---|---|---|---|---|---|
| AVDDA1 | 1.8 | BLM18HE601SN1D | Murata | 200 mA | 470 ohms or greater @ 100 MHz** | 250 mohms or less |
| AVDDA2 | 1.8 | BLM18HE601SN1D | Murata | 200 mA | 470 ohms or greater @ 100 MHz** | 250 mohms or less |
| AVDDA3 | 1.8 | BLM18HE601SN1D | Murata | 200 mA | 470 ohms or greater @ 100 MHz** | 250 mohms or less |
| DVDD18 | 1.8 | NFM18CC223R1C3 | Murata | 1000 mA | 65 dB @ ~140 MHz | 22,000 pF |
| VDDT1* | 1.0 | NFM18CC223R1C3 | Murata | 1000 mA | 65 dB @ ~140 MHz | 22,000 pF |
| VDDT2* | 1.0 | NFM18CC223R1C3 | Murata | 1000 mA | 65 dB @ ~140 MHz | 22,000 pF |
| VDDT3* | 1.0 | NFM18CC223R1C3 | Murata | 1000 mA | 65 dB @ ~140 MHz | 22,000 pF |
| CVDD1 | 1.0 | - | - | - | | - |
| CVDD | 1.0 | - | - | - | | - |
| VDDR1* | 1.5 | NFM18CC223R1C3 | Murata | 1000 mA | 65 dB @ ~140 MHz | 22,000 pF |

**Table 14 Power Rail Filter Recommendations (Part 2 of 2)**

| Power Rail | Voltage | Filter (p/n) | Mfg | Current | Insertion Loss (dB)/ Impedance | Capacitance/DCR |
|---|---|---|---|---|---|---|
| VDDR2* | 1.5 | NFM18CC223R1C3 | Murata | 1000 mA | 65 dB @ ~140 MHz | 22,000 pF |
| VDDR3* | 1.5 | NFM18CC223R1C3 | Murata | 1000 mA | 65 dB @ ~140 MHz | 22,000 pF |
| VDDR4* | 1.5 | NFM18CC223R1C3 | Murata | 1000 mA | 65 dB @ ~140 MHz | 22,000 pF |
| VDDR5* | 1.5 | NFM18CC223R1C3 | Murata | 1000 mA | 65 dB @ ~140 MHz | 22,000 pF |
| VDDR6* | 1.5 | NFM18CC223R1C3 | Murata | 1000 mA | 65 dB @ ~140 MHz | 22,000 pF |
| DVDD15 | 1.5 | - | - | - | | - |
| VREFSSTL | 0.75 | - | - | - | | - |
| **End of Table 14** | | | | | | |

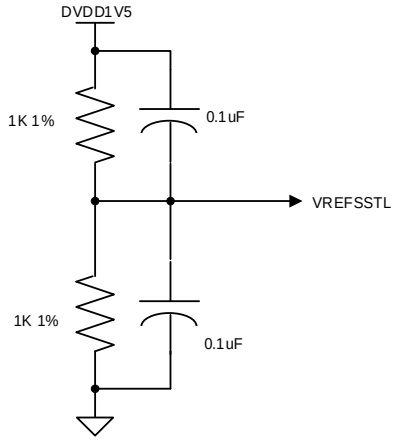
Note *: Filter not required if peripheral not used.
Note **: Requires the addition of a 100 nF and 10 nF ceramic capacitor between the ferrite and respective device pins. Routing must be kept short and clean.

## 5.4 Power Supply Reference Voltages

The C66x device requires a reference voltage for the DDR3 SDRAM interface. The use of a simple voltage divider as illustrated in Figure 16 is recommended. All resistive components must be 1% or better tolerance. The following figure must be placed close to the respective device pin.

The Vref source voltage MUST be generated from the same supply as the DRAM interface to the device (DVDD15). Both must track in parallel as the supply voltage fluctuates.

**Figure 16 DDR3 Vref Voltage Source**




## 5.5 Power Supply Layout Recommendations

Each core and I/O supply voltage regulators should be located close to the device (or device array) to minimize inductance and resistance in the power delivery path. Additional requirements include a separate power plane for the core, I/O, and ground rails, all bypassed with high-quality low-ESL/ESR capacitors. Refer to specific power supply data sheets for power plane requirements and support of specific power pads on each power supply.

A common DDR3 reference voltage divider should be used for both the C66x device and the reference voltage input on the SDRAMs. The VREF resistor divider should be placed between the device and DRAMs with interconnecting traces as short as possible and a minimum 20 mil wide. There should be a minimum 2× trace width clearance between the routing of the reference voltage and any switching signals.

## 5.6 Voltage Tolerances, Noise, and Transients

Voltage tolerances specified in the data sheet include all DC tolerances and the transient response (AC) of the power supply. These specify the absolute maximum levels that must be maintained at the pins of the C66x device under all conditions. Special attention to the power supply solution is needed to achieve this level of performance, especially the 5% tolerance on the core power plane (CVDD).

To maintain the 5% tolerance at the pins, the tolerance must be a combination of the power supply DC output accuracy and the effect of transients. A reasonable goal for the DC power supply output accuracy is 2.5%, leaving 2.5% for the transients. For example, at CVDD of 1.0 V, 5% tolerance is ±50 mV. This allows 25 mV of DC accuracy from the output of the power supply and another 25 mV due to AC transients.

### 5.6.1 Using Remote Sense Power Supplies

Unlike previous devices, the KeyStone I devices require high performance power solutions. Remote sensing power supplies can be used – however Texas Instruments has developed a solution specifically designed for the variable core rail for this device family (KeyStone I). The recommended solution (Section 5.7) is the only solution to be evaluated and guaranteed functional at this time. As others are evaluated they will be added to the acceptable list of approved supplies for the device variable core rail.

The recommended variable core supply supports voltage and current sense features and when designed in properly will meet all the HPMP device requirements.

## 5.7 Recommended Variable Core Supply

The following section defines the requirements for the KeyStone I variable (SmartReflex) supply. Many, if not most, applications require the use of multiple devices. For this reason, TI has developed a quad controller to support the variable core supply requirements.

**Note—**At the release of this document both a quad and dual version of the variable core supply are available. TI is working to develop and release other power supplies to meet other device requirements. This document will be continuously updated with alternate parts as they become available.

In a multi-processor system, power is critical. Voltage drop outside the tolerable ranges can render a design useless or account for performance goals not being met.

### 5.7.1 Recommended Components

To meet the rigorous demands of the C66x device, TI has developed and recommends several specific components to be used (*others under development and scheduled for release in the near future*). These include the UCD9244, or UCd9222, and the UCD7242, a quad or dual digital controller and dual output FET. As illustrated in the following figures, a

combination of these components will support up to four separate SmartReflex enabled device cores, or one core and three additional rails. Utilizing the recommend components each of the four outputs can support up to 10 amperes each continuously (20 amperes if UCD7242 outputs are tied together).

The UCD9244 digital controller allows for full control of all outputs (regardless of whether they are a fixed or a variable rail) and advanced features including the following:

- Switching frequencies up to 2 MHz
- Up To 1 mV Closed Loop Resolution
- Soft-Start and Soft-Stop
- Voltage tracking, margining and sequencing
- Input & output current and voltage control

Refer to the applicable data sheet for detailed implementation details not covered within this document.

Alternatively, for application hardware incorporating non-standard numbers of devices, TI offers a dual (2 output) digital controller (UCD9222). The functionality between the two controllers is almost identical with the exception of the two additional implicit outputs.

#### 5.7.1.1 Typical Core Logic Interconnections

The following series of figures illustrates four of the possible core power supply ⇔ device combinations available. These combinations take advantage of the newly developed core digital power controllers. The following figures illustrate different connectivity methods and emphasize the connectivity, additional bulk, and decoupling capacitance that may be required depending on use case. In all cases where the recommended digital controller (UCD92xx) is used, it will be necessary to complete the design and properly model it using the appropriate GUI design tool:

http://focus.ti.com/docs/toolsw/folders/print/fusion_digital_power_designer.html

Refer to the respective data sheets, application notes, user guides, and this document for additional details. TI continues to evolve its power supply support for the devices, so refer back to the product folder, this document, or your local FAE for additional details and updates.

The examples provided below are defined as follows:

1. A single dual output SmartReflex capable digital controller (UCD9222), a single dual output MOSFET (UCD7242), and two SmartReflex enabled devices (KeyStone I family) [Figure 17 & Figure 18], resulting in a maximum 10A per device variable core rail.
2. A single dual output SmartReflex capable digital controller (UCD9222), two dual output MOSFETs (UCD7242) with the outputs tied together for up to 2× the output current, and two SmartReflex enabled devices (KeyStone I family) [Figure 19, Figure 20, Figure 21], resulting in a maximum 20A per device variable core rail.
3. A single quad output SmartReflex capable digital controller (UCD9244), two dual output MOSFETs (UCD7242), and four SmartReflex enabled devices (KeyStone I family) [Figure 22 through Figure 24], resulting in a maximum 10 A per device variable core rail.

4. A single quad output SmartReflex capable digital controller (UCD9244), four dual output MOSFETs (UCD7242) with the outputs (of each) tied together for up to 2× the output current, and four SmartReflex enabled devices (KeyStone I family) [Figure 25 through Figure 27], resulting in a maximum 20 A per device variable core rail.

To prevent leakage current from accumulating on the variable core power rails, a 10K ohm resistor between each variable core power rail and ground is recommended. The following are examples of the core power supply, these examples are provided to illustrate connectivity, the amount of bulk capacitance will be based on individual topologies, component selections and power requirements (use cases). These examples to do not include decoupling or bypass capacitors which are needed and must be calculated. A minimum amount of bulk and decoupling capacitance is provided in this design guide as a reference.

The following two figures illustrate the connectivity where two devices, a single dual output digital controller, and a single dual output MOSFET exist. The resulting available current is 10 A per rail.

**Figure 17** **1-UCD9222 / 1-UCD7242 / 2-DSPs / 10 A each (1 of 2)**

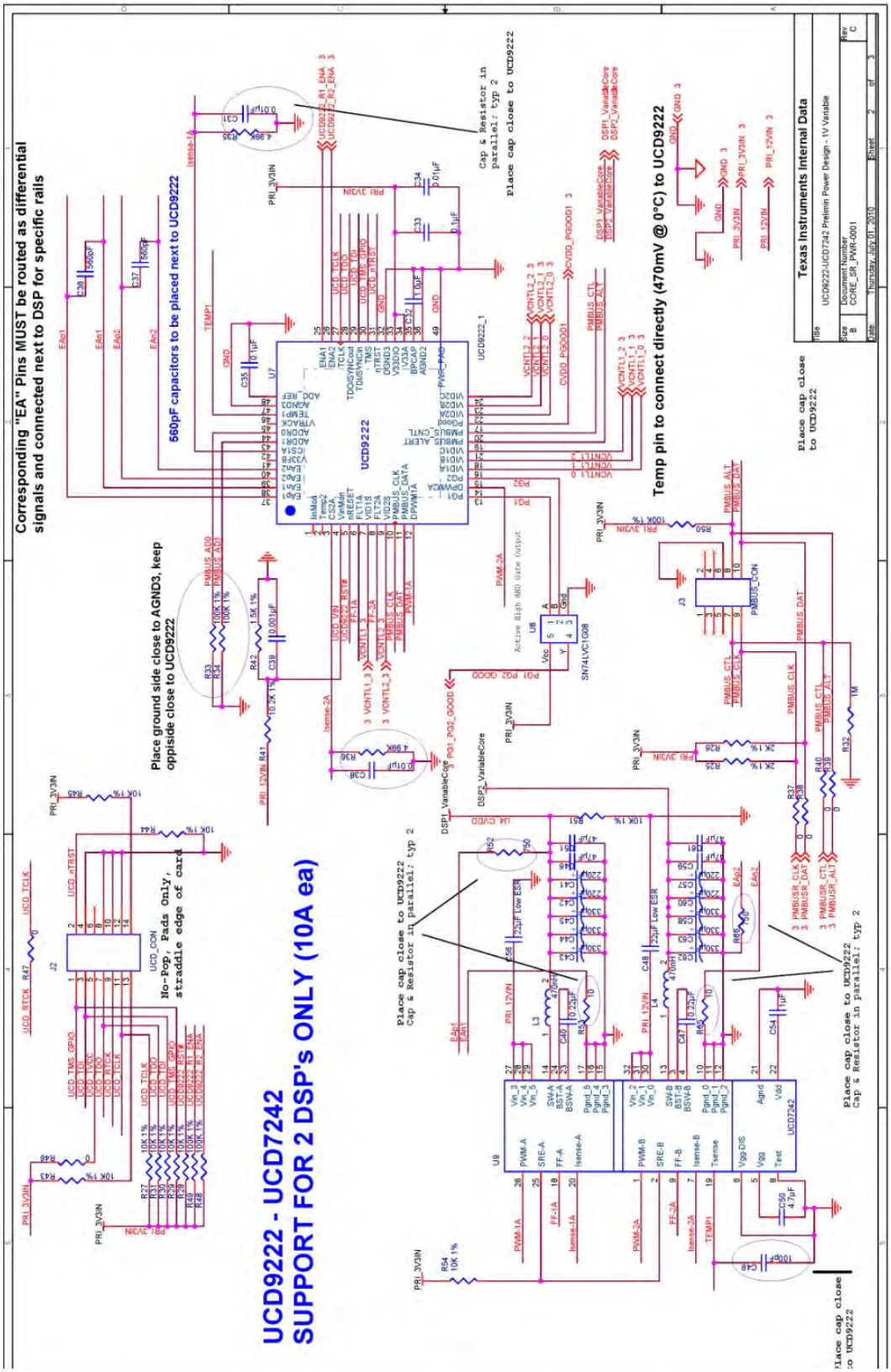
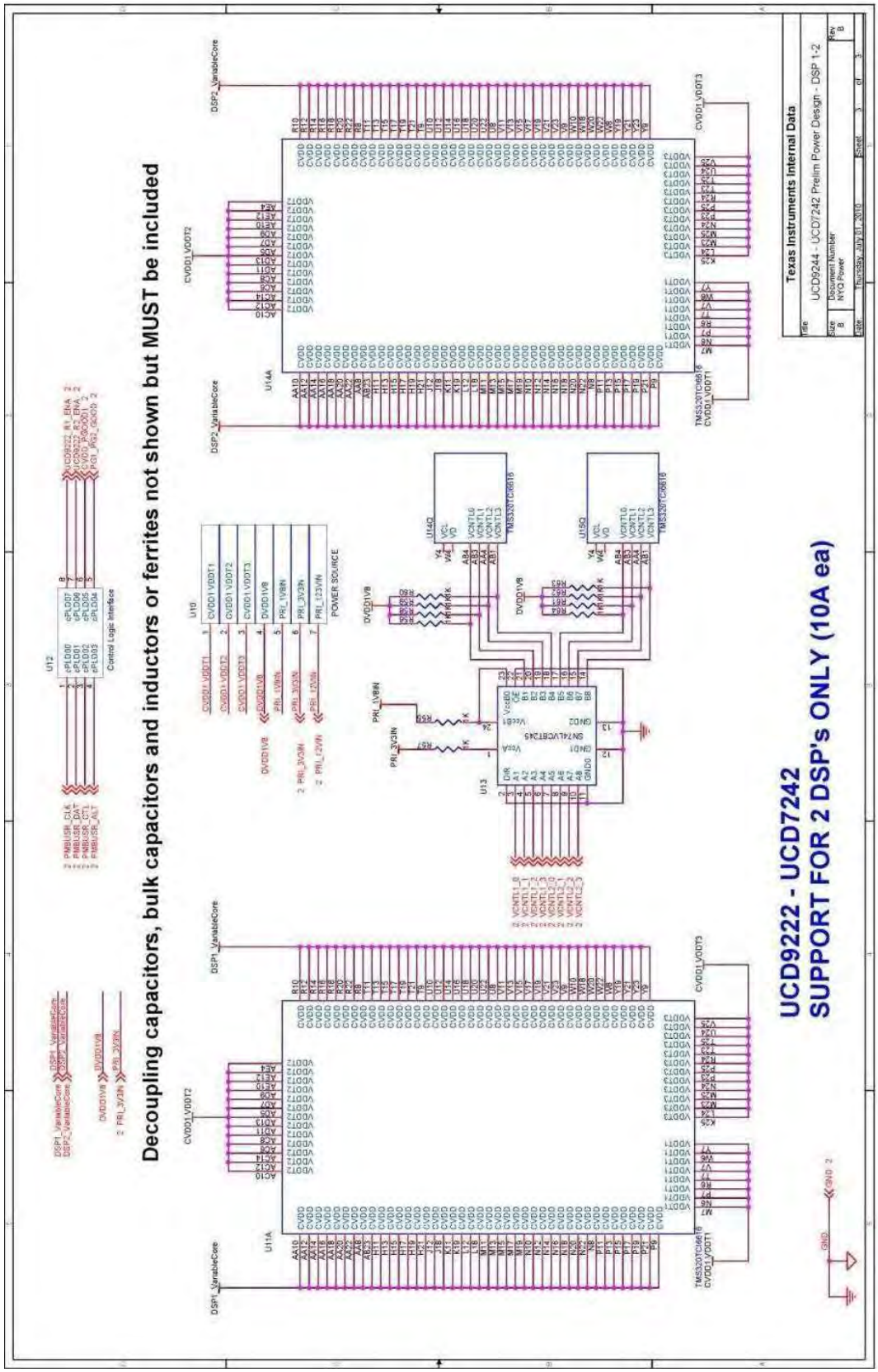


**Figure 18** **1-UCD9222 / 1-UCD7242 / 2-DSPs / 10 A each (2 of 2)**



The following three figures illustrate the connectivity where two DSPs exist, a single dual output digital controller and two dual output MOSFETs (outputs tied together to increase available current). The resulting available current is 20 A per rail.

**Figure 19** **1-UCD9222 / 2-UCD7242 / 2-DSPs / 20 A each (1 of 3)**

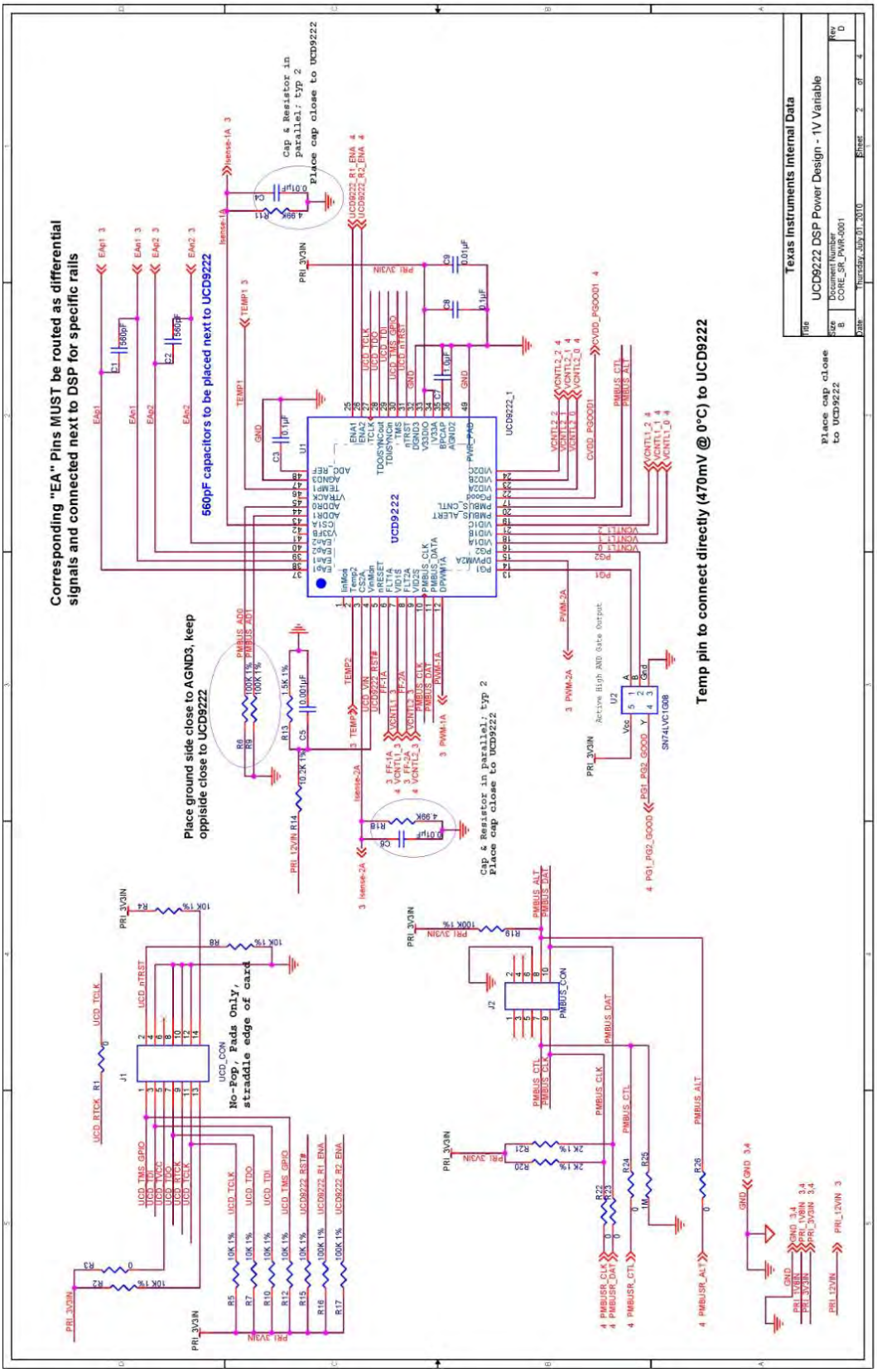


**Figure 20** **1-UCD9222 / 2-UCD7242 / 2-DSPs / 20 A each (2 of 3)**

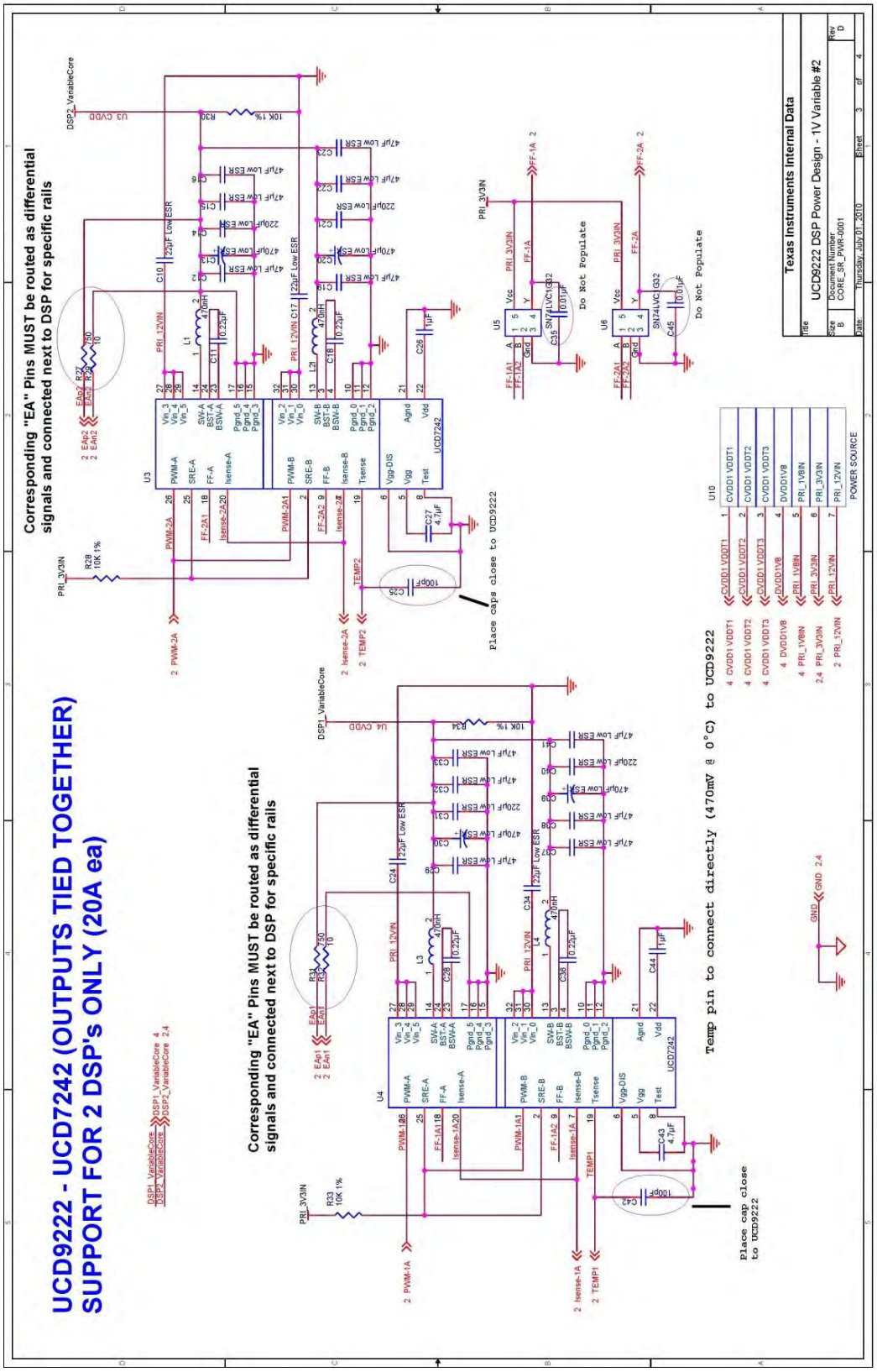
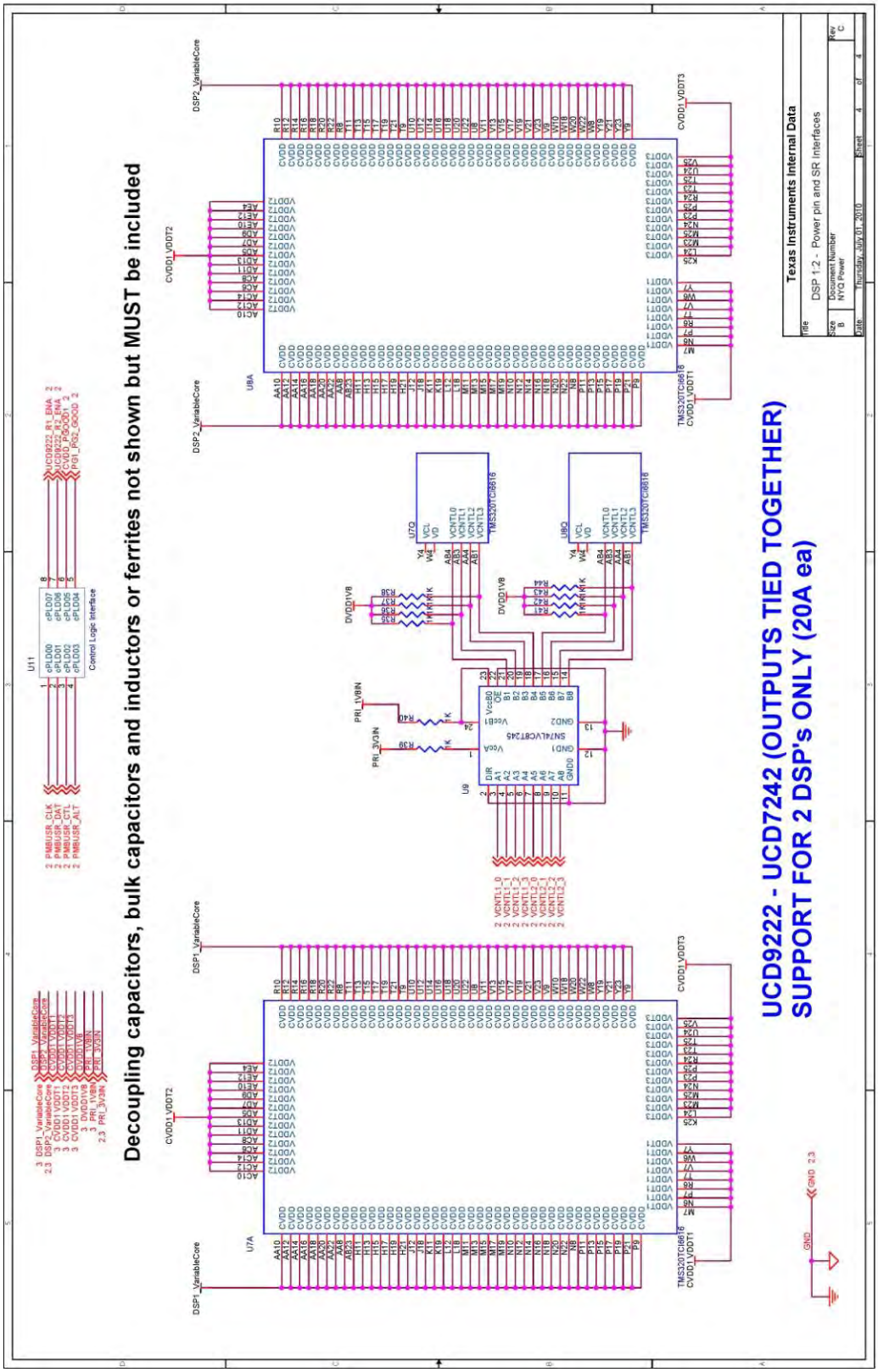


**Figure 21** **1-UCD9222 / 2-UCD7242 / 2-DSPs / 20 A each (3 of 3)**



The following three figures illustrate the connectivity where four DSPs exist, a single quad output digital controller and two dual output MOSFETs resulting in an available current of 10 A per rail.

**Figure 22** **1-UCD9244 / 2-UCD7242 / 4-DSPs / 10 A each (1 of 3)**

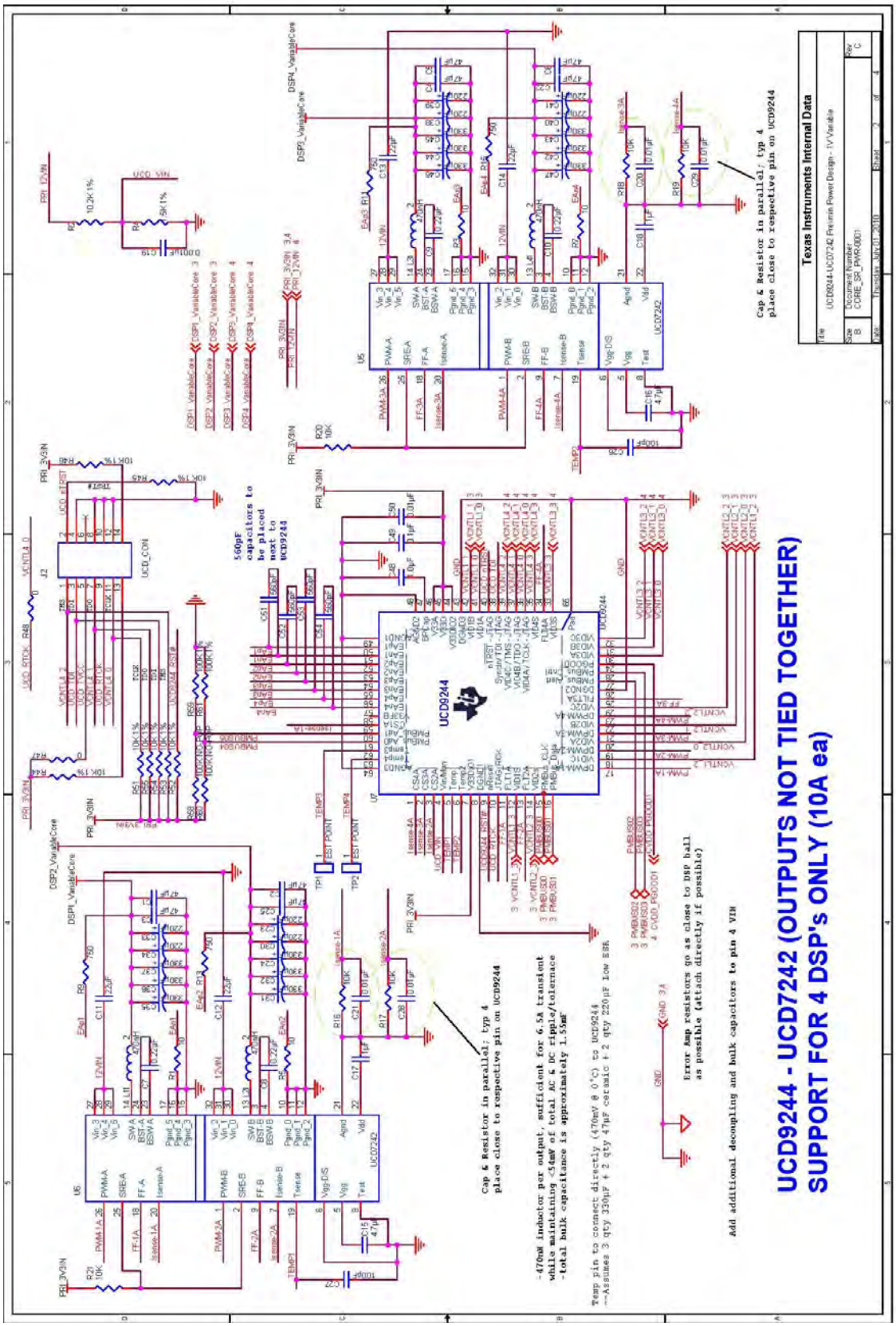


**Figure 23** **1-UCD9244 / 2-UCD7242 / 4-DSPs / 10 A each (2 of 3)**

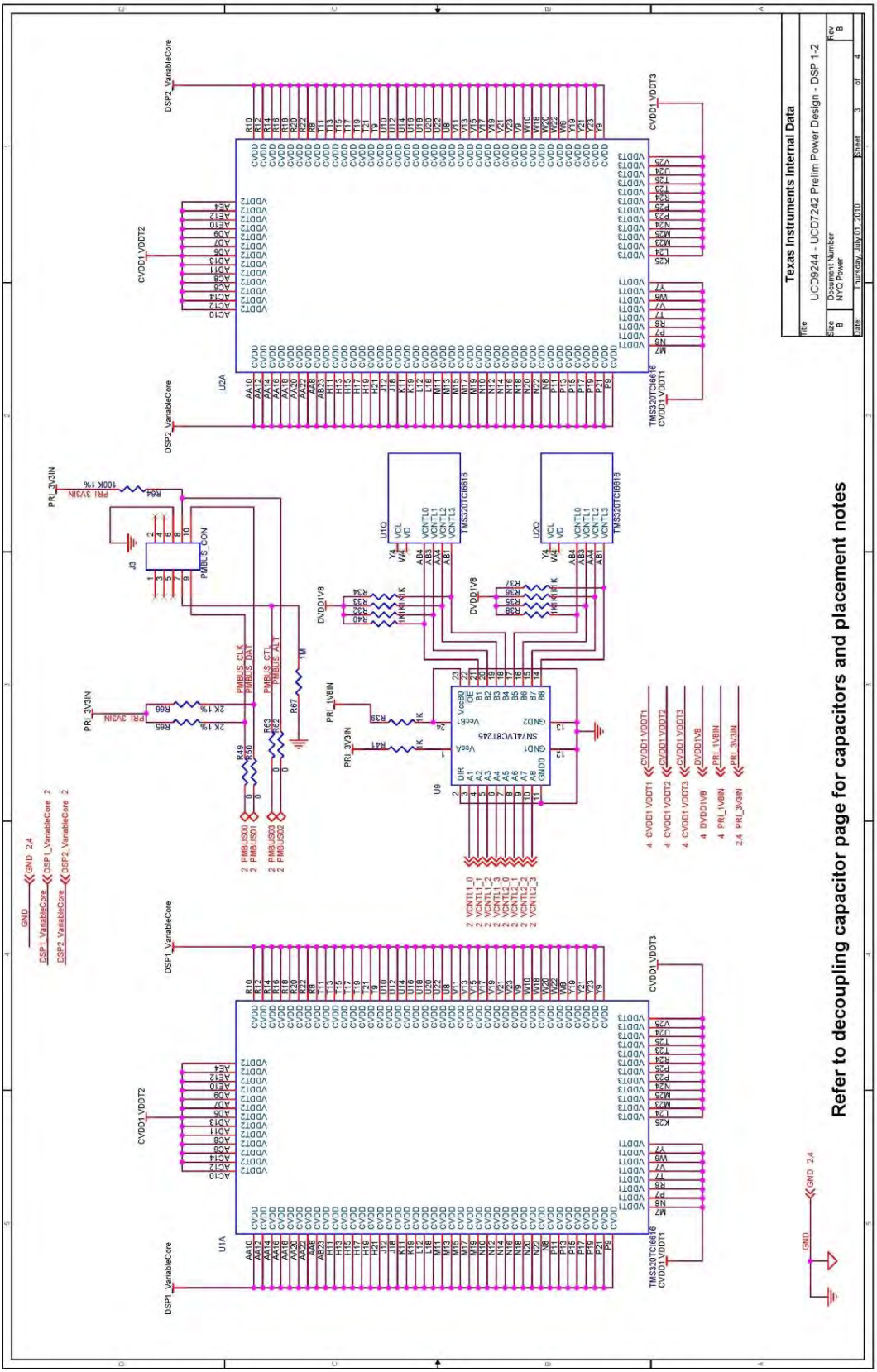
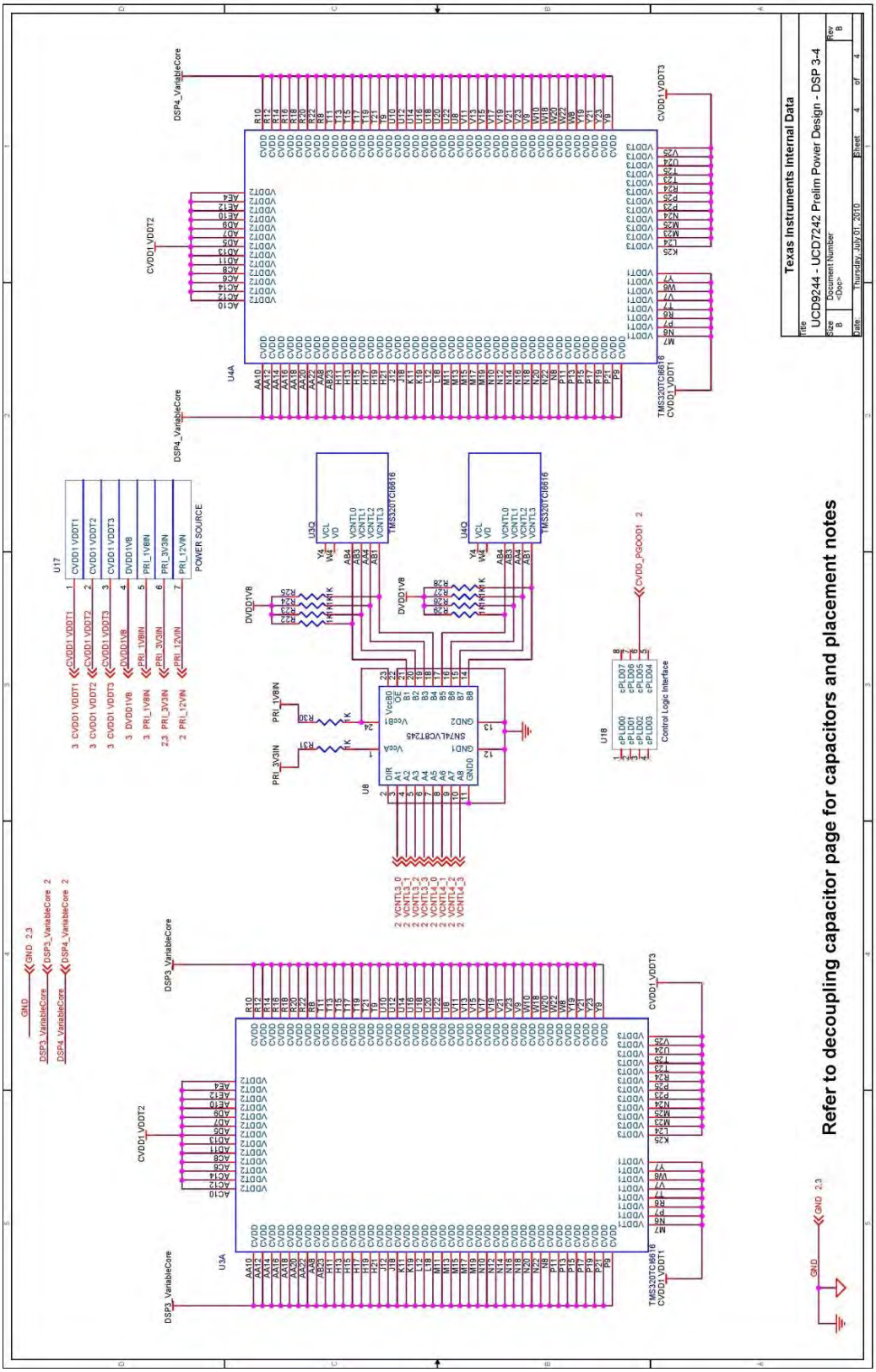


**Figure 24 1-UCD9244 / 2-UCD7242 / 4-DSPs / 10 A each (3 of 3)**



The following three figures illustrate the connectivity where four DSPs exist, a quad output digital controller and four dual output MOSFETs (outputs tied together to increase available current) resulting in an available current of 20 A per rail.

**Figure 25** **1-UCD9244 / 4-UCD7242 / 4-DSPs / 20 A each (1 of 3)**

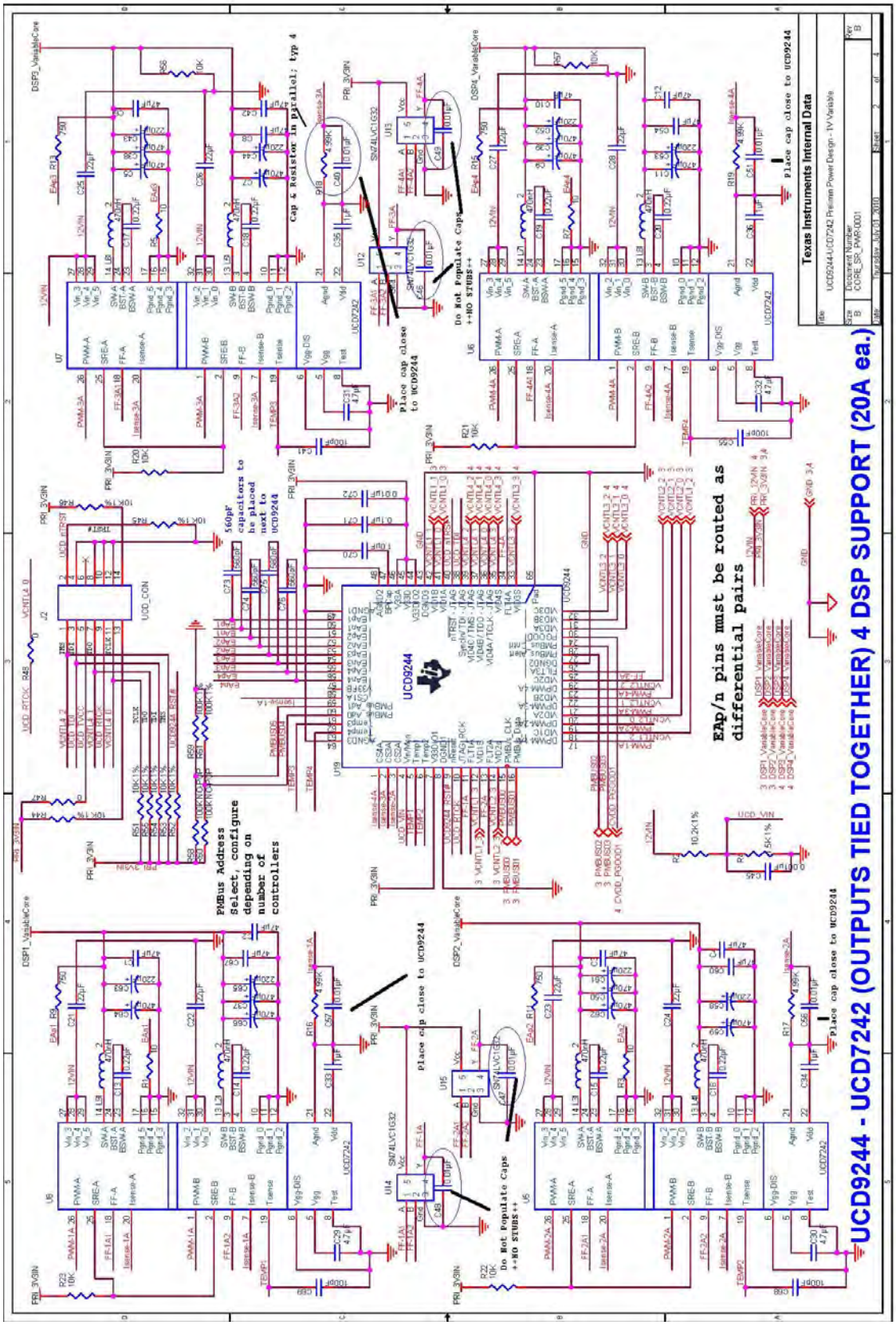


**Figure 26 1-UCD9244 / 4-UCD7242 / 4-DSPs / 20 A each (2 of 3)**

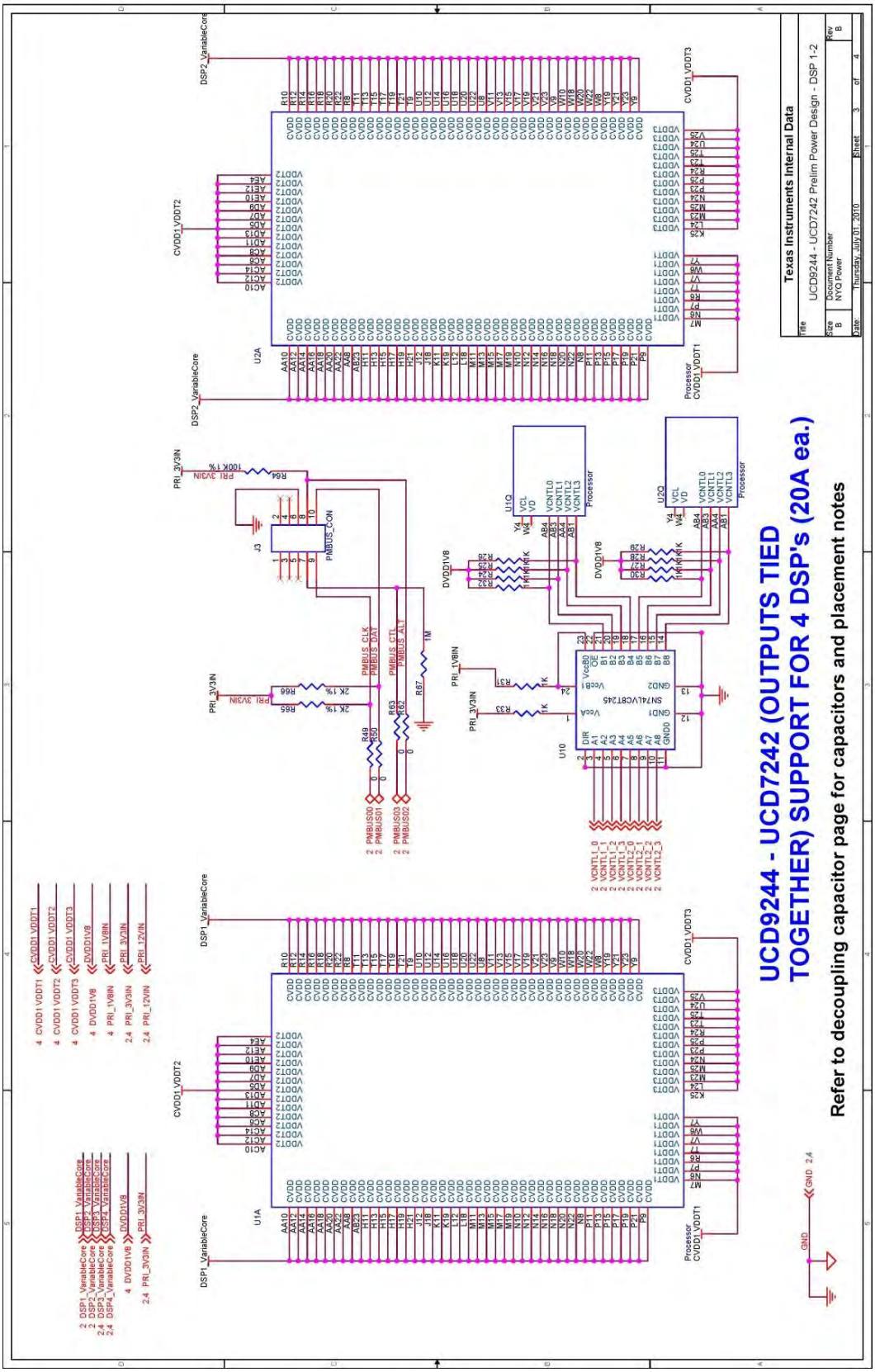
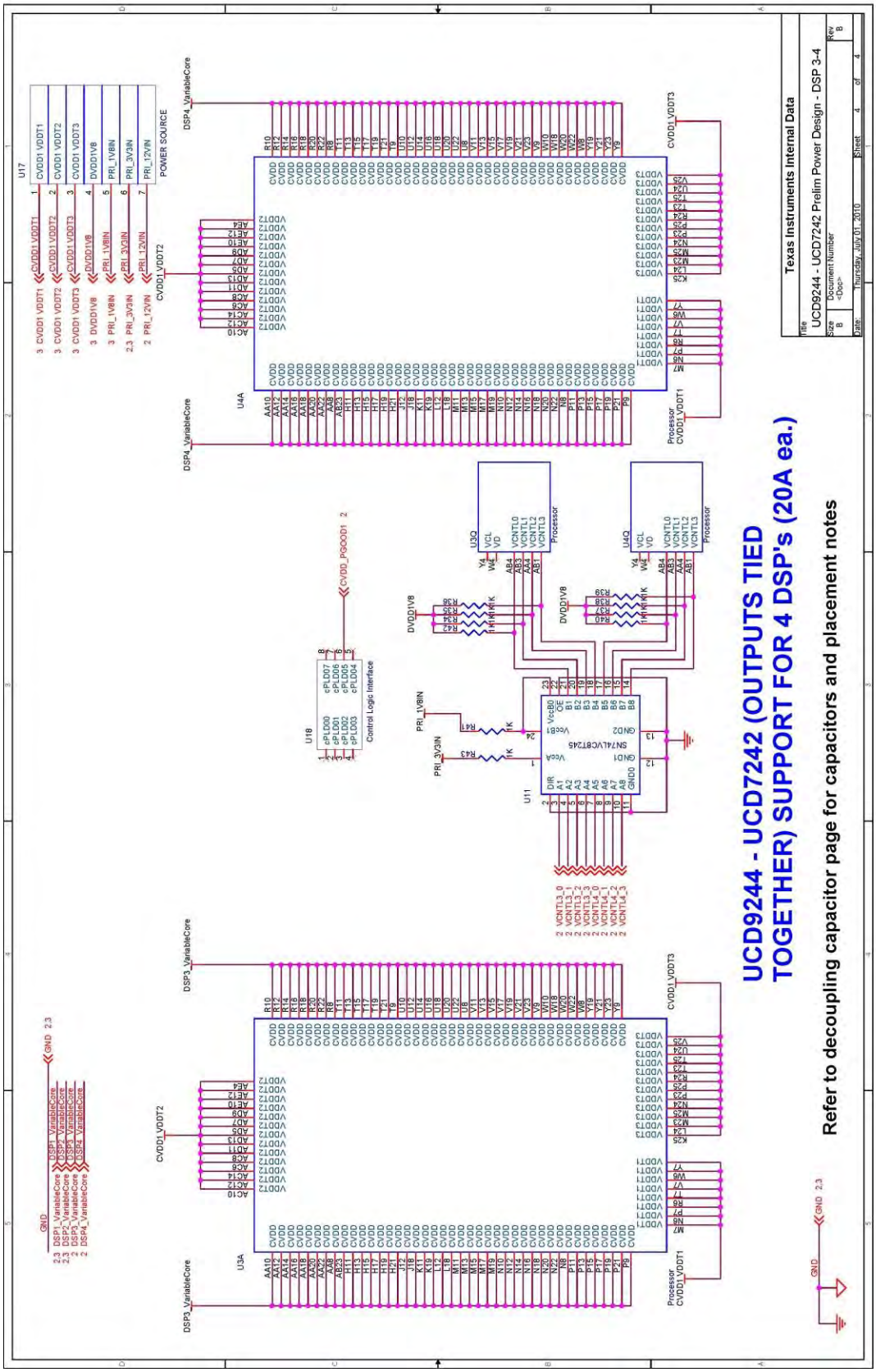


**Figure 27** **1-UCD9244 / 4-UCD7242 / 4-DSPs / 20 A each (3 of 3)**



## 5.8 Power-Supply Decoupling and Bulk Capacitors

To properly decouple the supply planes from system noise, decoupling and bulk capacitors are required. Component parasitics play an important role on how well noise is decoupled, for this reason bulk capacitors should be of the low ESR/ESL type and all decoupling capacitors (unless otherwise specified) should be ceramic and 0402 size (largest recommended). As always, power rating and component and PCB parasitics must be taken into account when developing a successful power supply system. Proper board design and layout allow for correct placement of all capacitors (refer to the reference table in Section 5.8.4 for a minimum set of capacitor recommendations and values).

Bulk capacitors are used to minimize the effects of low frequency current transients (see Section 5.8.1) and decoupling or bypass capacitors are used to minimize higher frequency noise (see Section 5.8.3). Proper printed circuit board design is required to assure functionality and performance.

One key element to consider during the circuit board (target) design is added lead inductance or the pad-to-plane length. Where possible, attachment for decoupling and bypass capacitors to the respective power plane should be made using multiple vias in each pad that connects the pad to the respective plane. The inductance of the via connect can eliminate the effectiveness of the capacitor so proper via connections are important. Trace length from the pad to the via should be no more than 10 mils (0.01") or 0.254 mm and the width of the trace should be the same width as the pad.

As with selection of any component, verification of capacitor availability over the product's production lifetime should be considered. Additionally the effects of the intended operating environment (temperature, humidity, etc.) should also be considered when selecting the appropriate decoupling and bulk capacitors.

**Note—**All values and recommendations are based on a single C66x device, TI high performance SWIFT power supplies and the New UCD9222/44 digital controller. The use of alternate non specified on-board power supply modules, alternate power supplies and alternate decoupling/bulk capacitor values and configurations require additional evaluation.

For further information in determining the minimal amount of bulk and decoupling capacitance required refer to the applicable spreadsheet.

### 5.8.1 Selecting Bulk Capacitance

The following subsection defines the key considerations necessary to select the appropriate bulk capacitors for each rail:

- Effective impedance for the power plane to stay within the voltage tolerance
- Amount of capacitance needed to provide power during the entire period when the voltage regulator cannot respond (sometimes referred to as the transient period)

The effective impedance of the core power plane is determined by:

(Allowable Voltage Deviation due to Current Transients) / (Max Current)

Calculating for the variable core supply, (*as an example only*) the allowable deviation (transient tolerance) is 25 mV (based on 2.5% AC [ripple] and 2.5% DC tolerance [voltage]) of the nominal 1 Vdc rail. Using an allowable 25 mV tolerance and a max transient current of 10 amps, the maximum allowable impedance can be calculated as follows:

25 mV/10 Amps = 2.5 mΩ

The effective ESR for all bulk capacitors (in the above example) should not exceed this impedance value. The combination of good quality and multiple bulk capacitors in parallel help to achieve the overall ESR required. Therefore, to limit the maximum transient voltage to a peak deviation of 25 mV, the power supply output impedance, which is a function of the power supply bandwidth and the low impedance output capacitance, should not exceed 2.5 mΩ.

The following three plots illustrate the recommended maximum impedance to current transient for three different tolerances (15 mV, 25 mV, and 35 mV). The first plot covers an allowable current between 500 mA to 3500 mA; the second plot covers 3700 mA to 6900 mA, and the final plot covers 7000 mA to 13000 mA.

**Figure 28 ESR Plot for Delta Current to Tolerance #1**

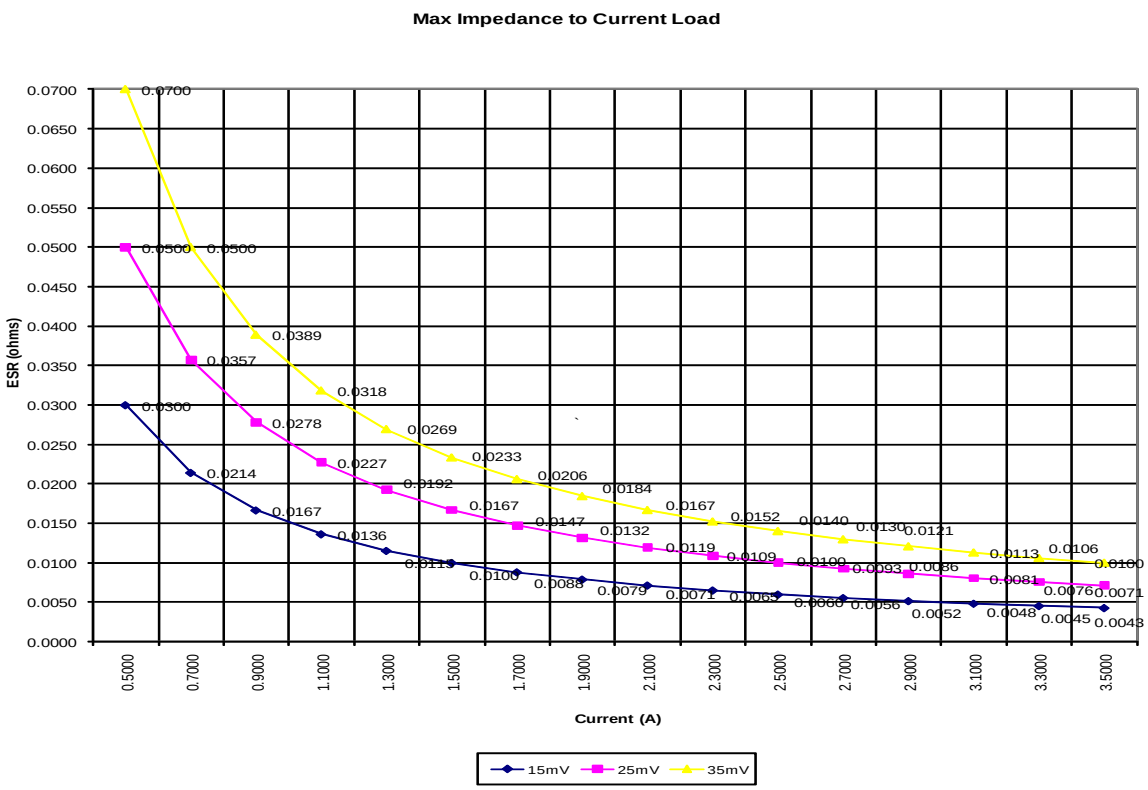


**Figure 29 ESR Plot for Delta Current to Tolerance #2**

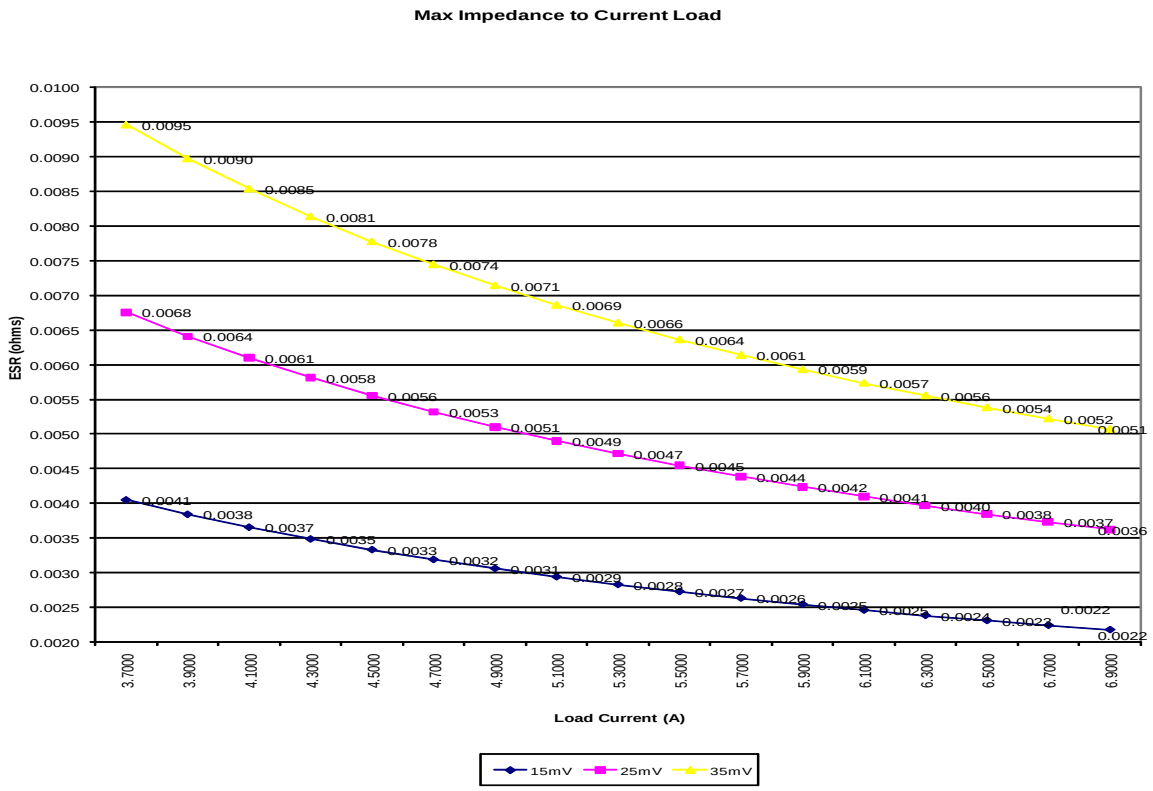
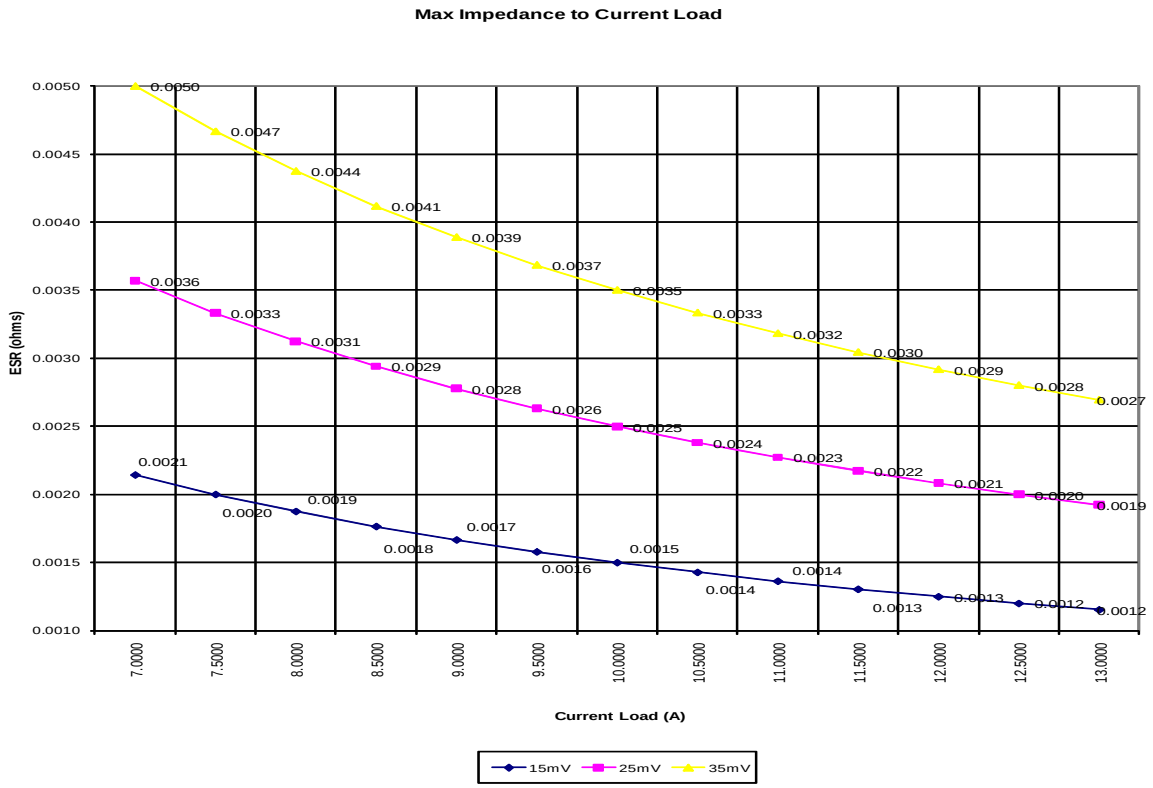



**Figure 30 ESR Plot for Delta Current to Tolerance #3**



The expected maximum current for the KeyStone I device (core) will depend heavily on the use case and design of the application hardware. The recommended components are designed to support to 17 A (at 86% efficiency) and up to 19 A when using the recommended components and implementing them correctly at 86% efficiency. It does not include current transients that occur during power on (yet these must be considered). Given the recommended topology only a reduced amount of bulk capacitors is possible provided they are chosen for there ESR/ESL and voltage rating properly. The majority of all core bulk capacitors must be located in close proximity to the UCD7242 Dual FETs.

Capacitance values should not be less than those specified in the applicable table under Section 5.8.4. Final capacitor selection is determined using the provided capacitor selection tool (see spreadsheet and application note).

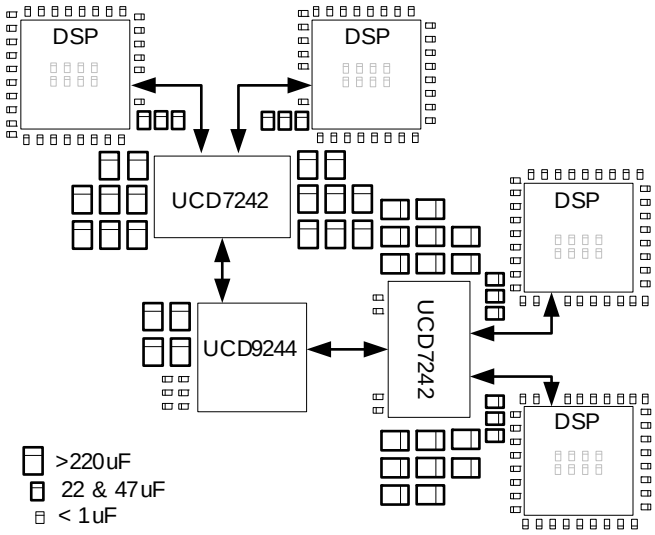
Some intermediate size ceramic bulk capacitors (i.e., 22 µF and 47 µF as listed under Section 5.8.2) are recommended to cover the response time between the bypass capacitors and the larger bulk capacitors.

#### 5.8.1.1 Bulk Capacitor Details and Placement

All bulk capacitors should be placed in close proximity to the respective power supply. Figure 31 illustrates the recommended placement (not quantity) for all core supply capacitors (core shown only). Should your topology or number of devices differ general design guidelines always apply (bulk capacitors as close to the respective power supplies and decoupling capacitors on the target device pins or as close as possible).

For the purpose of this document and related devices, a bulk capacitor is defined as any capacitor ≥ 22 µF unless otherwise noted.

**Figure 31 Recommended Core Bulk Capacitor Placement**




### 5.8.2 Selecting Intermediate Value Capacitors

All intermediate capacitors must be positioned as close to the device as possible, decoupling capacitors taking precedence where placement between the two form factors and values come into question. Intermediate capacitor values are considered those between 22 µF and 47 µF, they are low ESR and ceramic where possible.

### 5.8.3 Selecting Decoupling Capacitors

All decoupling or bypass capacitors must be positioned close to the device. In practice each decoupling capacitor should be placed 10mm maximum distance from the respective pin(s). Where possible each decoupling capacitor should be tied directly between the respective device pin and ground without the use of traces. Any parasitic inductance limits the effectiveness of the decoupling capacitors; therefore, the physically smaller the capacitors are (0402 or 0201 are recommended) the better the power supply will function.

Proper capacitance values are also important. All small decoupling or bypass capacitors (560 pF, 0.001 µF, 0.01 µF, & 0.1 µF) must be placed closest to the respective power pins on the target device. Medium bypass caps (100 nF or as large as can be obtained in a small package such as an 0402) should be the next closest. TI recommends placing decoupling capacitors immediately next to the BGA vias, using the *interior* BGA space and at least the corners of the *exterior*.

The inductance of the via connect can eliminate the effectiveness of the capacitor so proper via connections are important. Trace length from the pad to the via should be no more than 10 mils and the width of the trace should be the same width as the pad. If necessary, placing decoupling capacitors on the back side of the board is acceptable provided the placement and attachment is designed correctly.

#### 5.8.3.1 Decoupling Capacitor Details and Placement

All decoupling capacitors should be placed in close proximity to the device power pins. For the purpose of this document and related devices, a decoupling or bypass capacitor shall be defined as any capacitor < 1 µF unless otherwise noted.

Table 15 is intended to provide a minimum recommended decoupling capacitor value. Each decoupling or bypass capacitor should be directly coupled to the device via. Where direct coupling is impractical, use a trace 10 mil (0.010"/0.254 mm) or shorter, and having the same width as the capacitor pad is strongly recommended. The following values are minimums, many variables will have an affect on the performance of the power supply system. Re-evaluate the individual power supply design for all variables before implementing the final design.

### 5.8.4 Example Capacitance

Table 15 establishes the bulk and decoupling capacitance requirements for the various device voltage rails. In many cases these rails originate from a common source which accounts for a reduction in bulk capacitance for many rails. This table does not cover the additional capacitance (decoupling or bulk) required by any other components or the filters outlined in previous sections. All capacitance identified assumes the use of the recommended power supplies (especially for the variable core), and switching frequencies as indicated (refer to note section). The recommended values are in addition to those required for proper operation of the recommended power supplies.

The values identified in the following table are “per device” and assume a typical loading per device IO. In the event multiple devices are used and a voltage rail is common or shared (where applicable), the capacitor requirements must be re-evaluated (on a case by case basis) and take into account key concepts including current (load), minimum and maximum current requirements, voltage step, power supply switching frequency, and component ESR (other constraints also apply).

**Table 15 Bulk, Intermediate, & Bypass Capacitor Recommendations (abs. minimums) (Part 1 of 3)**

| Voltage Supply | Capacitors | Qty | ESR (m Ohms)* | Total Capacitance[5] | Description | Notes |
|---|---|---|---|---|---|---|
| $C_{VDD}$*** | 560 pF Ceramic | 20 | | 1662.9112 µF | Variable Core | 1, 5, 6, 12 |
| | 100 nF Ceramic | 8 | | | Supply | 5, 6, 12 |
| | 10 nF Ceramic | 10 | | | | 5, 6, 12 |
| | 22 µF Low ESR | 1 | 9m ohms* | | | 14 |
| | 47 µF Low ESR | 4 | 3m ohms* | | | 5, 6, 12 |
| | 47 µF Low ESR | 2 | 3m ohms* | | | 14 |
| | 220 µF Low ESR | 2 | 7m ohms* | | | 5, 6, 12 |
| | 330 µF Low ESR | 0 | | | | |
| | 470 µF Low ESR | 2 | 12m ohms* | | | 5, 6, 12 |
| $A_{VDDA}1$ | 560 pF Ceramic | 1 | | 72.81056 µF | 1.8 V Core PLL | 5, 6, 12 |
| | 100 nF Ceramic | 1 | | | Supply | 5, 6, 12 |
| | 10 nF Ceramic | 1 | | | | 5, 6, 12 |
| | 1 µF Ceramic | 0 | | | | |
| | 4.7 µF Ceramic | 1 | 10m ohms* | | | 5, 6, 12 |
| | 10 µF Ceramic | 0 | | | | |
| | 68 µF Ceramic | 1 | 2m ohms* | | | 5, 6, 12 |
| $A_{VDDA}2$ | 560 pF Ceramic | 1 | | 26.81056 µF | 1.8V DDR3 PLL | 5, 6, 12 |
| | 100 nF Ceramic | 1 | | | Supply | 5, 6, 12 |
| | 10 nF Ceramic | 1 | | | | 5, 6, 12 |
| | 1 µF Ceramic | 0 | | | | |
| | 4.7 µF Ceramic | 1 | 10m ohms* | | | 5, 6, 8, 12 |
| | 10 µF Ceramic | 0 | | | | |
| | 22 µF Ceramic | 1 | 10m ohms* | | | 5, 6, 8, 12 |
| $A_{VDDA}3$ | 560 pF Ceramic | 1 | | 26.81056 µF | 1.8V PLL | 5, 6, 12 |
| | 100 nF Ceramic | 1 | | | Supply | 5, 6, 12 |
| | 10 nF Ceramic | 1 | | | | 5, 6, 12 |
| | 1 µF Ceramic | 0 | | | | |
| | 4.7 µF Ceramic | 1 | 10m ohms* | | | 5, 6, 8,12 |
| | 10 µF Ceramic | 0 | | | | |
| | 22 µF Ceramic | 1 | 10m ohms* | | | 5, 6, 8, 12 |
| $D_{VDD}18$ | 560 pF Ceramic | 8 | | 125.03748 µF | 1.8V IO | 2, 5, 6, 12 |
| | 100 nF Ceramic | 3 | | | Supply | 2, 5, 6, 12 |
| | 10 nF Ceramic | 3 | | | | 2, 5, 6, 12 |
| | 1 nF Ceramic | 3 | | | | 2, 5, 6, 12 |
| | 1 µF Ceramic | 0 | | | | |
| | 4.7 µF Ceramic | 1 | 10m ohms* | | | 2, 5, 6, 12 |
| | 10 µF Ceramic | 2 | 9m ohms* | | | 2, 5, 6, 12 |
| | 47 µF Low ESR | 0 | | | | |
| | 100 µF Low ESR | 1 | 9m ohms* | | | 2, 5, 6, 12 |
| | 220 µF Low ESR | 0 | | | | |
| VDDT1 | 560 pF Ceramic | 2 | | 15.81212 µF | 1.0V MCM | 5, 6, 12 |
| | 100 nF Ceramic | 1 | | | Termination | 5, 6, 12 |
| | 10 nF Ceramic | 1 | | | Supply | 5, 6, 12 |

**Table 15 Bulk, Intermediate, & Bypass Capacitor Recommendations (abs. minimums) (Part 2 of 3)**

| Voltage Supply | Capacitors | Qty | ESR (m Ohms)* | Total Capacitance[5] | Description | Notes |
|---|---|---|---|---|---|---|
| | 1 µF Ceramic | 1 | 12m ohms* | | | 5, 6, 9, 12 |
| | 4.7 µF Ceramic | 1 | 10m ohms* | | | 5, 6, 12 |
| | 10 µF Ceramic | 1 | 9m ohms* | | | 5, 6, 9, 12 |
| VDDT2 | 560 pF Ceramic | 3 | | 1.13168 µF | 1.0V SGMII/ | 5, 6, 12 |
| | 100 nF Ceramic | 1 | | | SRIO/PCIe | 5, 6, 12 |
| | 10 nF Ceramic | 2 | | | Termination | 5, 6, 12 |
| | 1 µF Ceramic | 1 | 12m ohms* | | Supply | 5, 6, 12 |
| | 4.7 µF Ceramic | 1 | 10m ohms* | | | 5, 6, 12, 15 |
| | 10 µF Ceramic | 0 | | | | 9 |
| VDDT3 | 560 pF Ceramic | 3 | | 1.13168 µF | 1.0V AIF | 5, 6, 12 |
| | 100 nF Ceramic | 1 | | | Termination | 5, 6, 12 |
| | 10 nF Ceramic | 1 | | | Supply | 5, 6, 12 |
| | 1 µF Ceramic | 1 | 12m ohms* | | | 5, 6, 12 |
| | 4.7 µF Ceramic | 1 | 10m ohms* | | | 5, 6, 12, 15 |
| | 10 µF Ceramic | 0 | | | | 9 |
| $C_{VDD}1$ | 560 pF Ceramic | 10 | | 277.4556 µF | 1.0 V Fixed | 3, 5, 6, 12 |
| | 100 nF Ceramic | 4 | | | Supply | 3, 5, 6, 12 |
| | 10 nF Ceramic | 5 | | | | 3, 5, 6, 12 |
| | 1 µF Ceramic | 0 | | | | |
| | 10 µF Ceramic | 3 | 9m ohms* | | | 14 |
| | 47 µF Low ESR | 1 | 3m ohms* | | | 3, 5, 6, 12 |
| | 100 µF Low ESR | 2 | 9m ohms* | | | 3, 5, 6, 12 |
| | 220 µF Low ESR | 0 | | | | |
| $D_{VDD}$1MCM | 560 pF Ceramic | 1 | | 1.02156 µF | 1.5 V MCM | 5, 6, 12 |
| | 100 nF Ceramic | 0 | | | Supply | |
| | 10 nF Ceramic | 2 | | | | 5, 6, 12 |
| | 1 nF Ceramic | 1 | | | | 5, 6, 12 |
| | 1 µF Ceramic | 1 | | | | 13 |
| | 10 µF Low ESR | 0 | | | | |
| $D_{VDD}$2PCIe | 560 pF Ceramic | 1 | | 1.02156 µF | 1.5 V PCIe | 5, 6, 12 |
| | 100 nF Ceramic | 0 | | | Supply | |
| | 10 nF Ceramic | 2 | | | | 5, 6, 12 |
| | 1 nF Ceramic | 1 | | | | 5, 6, 12 |
| | 1 µF Ceramic | 1 | 12m ohms* | | | 13 |
| | 10 µF Low ESR | 0 | | | | |
| $D_{VDD}$3SGMII | 560 pF Ceramic | 1 | | 1.02156 µF | 1.5 V SGMII | 5, 6, 12 |
| | 100 nF Ceramic | 0 | | | Supply | |
| | 10 nF Ceramic | 2 | | | | 5, 6, 12 |
| | 1 nF Ceramic | 1 | | | | 5, 6, 12 |
| | 1 µF Ceramic | 1 | 12m ohms* | | | 13 |
| | 10 µF Low ESR | 0 | | | | |
| $D_{VDD}$4SRIO | 560 pF Ceramic | 1 | | 1.02156 µF | 1.5 V SRIO | 5, 6, 12 |
| | 100 nF Ceramic | 0 | | | Supply | |

**Table 15 Bulk, Intermediate, & Bypass Capacitor Recommendations (abs. minimums) (Part 3 of 3)**

| Voltage Supply | Capacitors | Qty | ESR (m Ohms)* | Total Capacitance[5] | Description | Notes |
|---|---|---|---|---|---|---|
| | 10 nF Ceramic | 2 | | | | 5, 6, 12 |
| | 1 nF Ceramic | 1 | | | | 5, 6, 12 |
| | 1 µF Ceramic | 1 | 12m ohms* | | | 13 |
| | 10 µF Low ESR | 0 | | | | |
| $D_{VDD}$5AIF1 | 560 pF Ceramic | 1 | | 1.02156 µF | 1.5 V AIF | 5, 6, 12 |
| | 100 nF Ceramic | 0 | | | Supply | |
| | 10 nF Ceramic | 1 | | | | 5, 6, 12 |
| | 1 nF Ceramic | 1 | | | | 5, 6, 12 |
| | 1 µF Ceramic | 1 | 12m ohms* | | | 13 |
| | 10 µF Low ESR | 0 | | | | |
| $D_{VDD}$6AIF2 | 560 pF Ceramic | 1 | | 1.02156 µF | 1.5 V AIF | 5, 6, 12 |
| | 100 nF Ceramic | 0 | | | Supply | |
| | 10 nF Ceramic | 2 | | | | 5, 6, 12 |
| | 1 nF Ceramic | 1 | | | | 5, 6, 12 |
| | 1 µF Ceramic | 1 | 12m ohms* | | | 13 |
| | 10 µF Low ESR | 0 | | | | |
| $D_{VDD}$15 | 560 pF Ceramic | 8 | | 5.16448 µF | 1.5 V DDR | 4,5,6,10,12 |
| | 100 nF Ceramic | 4 | | | Supply | 4,5,6,10,12 |
| | 10 nF Ceramic | 6 | | | | 4,5,6,10,12 |
| | 1 nF Ceramic | 0 | | | | |
| | 1 µF Ceramic | 0 | | | | |
| | 4.7 µF Ceramic | 1 | 10m ohms* | | | 4,5,6,10,12 |
| | 10 µF Low ESR | 0 | | | | |
| | 22 µF Low ESR | 0 | | | | |
| | 47 µF Low ESR | 0 | | | | |
| | 100 µF Low ESR | 0 | | | | |
| | 220 µF Low ESR | 0 | | | | |
| VREFSSTL | 100 nF Ceramic | 2 | | 0.2000 µF | 1.5 V DDR $V_{REF}$ Supply | |
| TOTAL | | | | 2281.40528 µF | | |

Notes:
1. Estimates provided assume 10 W @ 1 V for the variable (scalable) core
2. Estimates provided assume 0.75 W @ 1.8 V for the 1.8 V IOs
3. Estimates provided assume 5 W @ 1 V for the fixed core
4. Estimates provided assume 1.0 W @ 1.5 V for the DDR3 IOs (SDRAM not included in estimations)
5. Always denotes a minimum capacitance
6. Fsw is 1e6 Hz.
7. Fsw is 550e3 Hz
8. Not required if common input to rail to supply (bulk is applied to AVDDA1)and distance is short between supply and device pin
9. Not required if adequate bulk capacitance is supplied for CVDD1 common input
10. Additional capacitance required when adding SDRAM (must be common supply per device)
11. To be placed on the input side of the ferrite or filter
12. Total value is calculated on a 1.5 pF device pin capacitance, variations in pin capacitance require re-calculation
13. Not required if adequate bulk capacitance is supplied for DVDD15 common input
14. Required for all devices within the same family having higher current requirements beyond that identified (future devices)
15. Not required if supplied for VDDT1 and is a common input source

Note: ***: capacitor selection for Cvdd variable core (as well as all other supplies) is highly dependant upon design and must be evaluated on a case by case scenario. The bulk capacitors shown are with respect to a 470 nH inductor for 10 A with a maximum delta current of 85%, other configurations may apply.

Note: *: refers to each individual capacitor ESR Value (and is a maximum value per capacitor)

**Note—**The capacitor values provided are a MINIMUM recommended amount.

Final capacitor value should not be less than the value specified in Section 5.8.4. Final selection for the core rails are determined using the provided capacitor selection tool and power estimation application guide which take into account the board impedance, variation in the $CV_{DD}$ supply voltage, use case, and the ESR of the bulk and decoupling capacitors selected.

#### 5.8.4.1 Calculating the Value of Bypass Capacitors

The following is a brief example of how the decoupling (bypass) capacitance was obtained. Final capacitor values should not be less than the values specified in Table 15. Final selection must take into account key variables including PCB board impedance, supply voltage, PCB topologies, component ESR, layout and design, as well as the end use application which should include cross talk and overall amount of AC ripple allowed.

#### 5.8.4.2 Guidelines for the calculation of decoupling capacitors

1. Assume all gates are switching at the same time (simultaneously) in the system, identify the maximum expected step change in power supply current $\Delta I$.
2. Estimate the maximum amount of noise that the system can tolerate.
3. Divide the noise voltage by the current change results in the maximum common path impedance or:

$$Z_{\max} = V_n / \Delta_I$$

4. Compute the inductance ( $L_{PSW}$ ) of the power supply wiring. Use this and the maximum common path impedance ( $Z_{\max}$ ) to determine the frequency,

$$f_{PSW} = f_{corner} = f_{3db} = Z_{\max} / (2\Pi L_{PSW})$$ below which the power supply wiring is fine (power supply wiring noise <$V_n$.

5. Calculate the capacitance ($C_{bypass}$) of the bypass capacitor:

$$C_{bypass} = 1/2\Pi * f_{PSW} * Z_{\max}$$

**Note—**If the operating frequency $f_{oper} \langle f_{PSW}$, then no bypass capacitor(s) are necessary. If $f_{oper} \geq f_{PSW}$ then bypass or decoupling capacitors are needed. The following example is provided as a sample calculation.

**Example**: (Decoupling Capacitance)

**Table 16 Total Decoupling Capacitance**

| Rail | Voltage | Pins | nF | Notes |
|---|---|---|---|---|
| CVDD | 1V0 | 81 | 773.490 | SmartReflex® Rail |
| AVDDA1 | 1V8 | 1 | 410.620 | |
| AVDDA2 | 1V8 | 1 | 14.3239 | |
| AVDDA3 | 1V8 | 1 | 14.3239 | |
| DVDD18 | 1V8 | 18 | 14.3239 | |
| VDDT1 | 1V0 | 8 | 14.3239 | |
| VDDT2 | 1V0 | 13 | 14.3239 | |
| VDDT3 | 1V0 | 12 | 14.3239 | |
| CVDD1 | 1V0 | 43 | 76.3944 | Fixed 1V rail |
| DVDD1MCM | 1V5 | 1 | 124.14 | |
| DVDD2PCIe | 1V5 | 1 | 114.5292 | |
| DVDD3SGMII | 1V5 | 1 | 17.1887 | |
| DVDD4SRIO | 1V5 | 1 | 17.1887 | |
| DVDD5AIF1 | 1V5 | 1 | 17.1887 | |
| DVDD6AIF2 | 1V5 | 1 | 444.042 | |
| DVDD15 | 1V5 | 31 | 309.397 | |
| VrefSSTL | 0V75 | 1 | 17.9049 | |
| **End of Table 16** | | | | |

Assumptions (Core):

- 81 core power pins
- 2.5% ripple allowed
- supply voltage is 1.0 V
- each pin has a capacitive load of 1.5 pF
- power supply inductance is 100 nH (approx. from PCB stack up)
- power supply switching frequency is 1000 kHz

1. Calculate the current: $\Delta I = nC * Vcc/\Delta t \rightarrow \Delta I = (81)(1.5^{-12})(1.0)/1^{-9} \rightarrow$

   $\Delta I = (1.066^{-10})/1^{-9} \rightarrow \Delta I = 0.1215$

2. Maximum impedance; $Z_{\max} = 25mV/0.1215 \rightarrow Z_{\max} = 0.205761316872\Omega$

3. Insert the power supply switching frequency: $f_{PSW} = 1000^3$
4. Calculate the bypass value(s) needed:

   $C_{bypass(\min)} = 1/(2 * \Pi * f_{PSW} * Z_{\max}) \rightarrow$

   $C_{bypass\ (\min)} = 1/(2 * pi * 1e6 * 0.2057613168\ \ 7242) \rightarrow$

   $C_{bypass(\min)} = 1/1292836.483 \rightarrow C_{bypass(\min)} = 7.7349302^{-7}$ or 0.77349302uF

In theory, decoupling capacitors should be placed on all pins, or at a minimum pins that share a common via to the power rail.

## 5.9 SmartReflex

In order to reduce device power, SmartReflex provides a feature that allows the core voltage to be optimized (scaled) based on the process corners of each device. Using the recommended UCD9244/7242 combination for the core, the C66x device can be regulated thereby reducing the overall power consumption. The current UCD9244/7242 configuration supports up to four separate DSPs. For systems where four DSPs are not required, the UCD9244/UCD7242 combination controller can be used to supply most fixed rails (1-scalable, 3-fixed). The C66x device has been designed to support SmartReflex Class 0 and Class 3. A brief description for each of these classes is provided in Section 5.9.3. Voltage selection is accomplished using four VCNTL pins that are used to select the output voltage of the core voltage regulator. The mapping of the VCNTL pins state to the $CV_{DD}1V0$ is shown in Table 17.

**Table 17 VCNTL Pin Mapping**

| VCNTL # | VCNTL (3:0) | VDD | | VCNTL # | VCNTL (3:0) | VDD |
|---|---|---|---|---|---|---|
| 0 | 00 0000b | 0.7 | | 32 | 10 0000b | 0.905 |
| 1 | 00 0001b | 0.706 | | 33 | 10 0001b | 0.911 |
| 2 | 00 0010b | 0.713 | | 34 | 10 0010b | 0.918 |
| 3 | 00 0011b | 0.719 | | 35 | 10 0011b | 0.924 |
| 4 | 00 0100b | 0.726 | | 36 | 10 0100b | 0.93 |
| 5 | 00 0101b | 0.732 | | 37 | 10 0101b | 0.937 |
| 6 | 00 0110b | 0.738 | | 38 | 10 0110b | 0.943 |
| 7 | 00 0111b | 0.745 | | 39 | 10 0111b | 0.95 |
| 8 | 00 1000b | 0.751 | | 40 | 10 1000b | 0.956 |
| 9 | 00 1001b | 0.758 | | 41 | 10 1001b | 0.962 |
| 10 | 00 1010b | 0.764 | | 42 | 10 1010b | 0.969 |
| 11 | 00 1011b | 0.77 | | 43 | 10 1011b | 0.975 |
| 12 | 00 1100b | 0.777 | | 44 | 10 1100b | 0.982 |
| 13 | 00 1101b | 0.783 | | 45 | 10 1101b | 0.988 |
| 14 | 00 1110b | 0.79 | | 46 | 10 1110b | 0.994 |
| 15 | 00 1111b | 0.796 | | 47 | 10 1111b | 1.001 |
| 16 | 01 0000b | 0.802 | | 48 | 11 0000b | 1.007 |
| 17 | 01 0001b | 0.809 | | 49 | 11 0001b | 1.014 |
| 18 | 01 0010b | 0.815 | | 50 | 11 0010b | 1.02 |
| 19 | 01 0011b | 0.822 | | 51 | 11 0011b | 1.026 |
| 20 | 01 0100b | 0.828 | | 52 | 11 0100b | 1.033 |
| 21 | 01 0101b | 0.834 | | 53 | 11 0101b | 1.039 |
| 22 | 01 0110b | 0.841 | | 54 | 11 0110b | 1.046 |
| 23 | 01 0111b | 0.847 | | 55 | 11 0111b | 1.052 |
| 24 | 01 1000b | 0.854 | | 56 | 11 1000b | 1.058 |
| 25 | 01 1001b | 0.86 | | 57 | 11 1001b | 1.065 |
| 26 | 01 1010b | 0.866 | | 58 | 11 1010b | 1.071 |
| 27 | 01 1011b | 0.873 | | 59 | 11 1011b | 1.078 |
| 28 | 01 1100b | 0.879 | | 60 | 11 1100b | 1.084 |
| 29 | 01 1101b | 0.886 | | 61 | 11 1101b | 1.09 |
| 30 | 01 1110b | 0.892 | | 62 | 11 1110b | 1.097 |
| 31 | 01 1111b | 0.898 | | 63 | 11 1111b | 1.103 |
| **End of Table 17** | | | | | | |

**Note—**Not all ranges or voltage levels are supported and should not be used, altered, or modified unless required per the respective data sheet or application notes. The intended range of operation is between 31 and 50 (0.905 V – 1.020 V), operation outside this range may impact device reliability or performance.

### 5.9.1 SmartReflex VCNTL Interface

The VCNTL pins of the device and UCD9244 require the addition of a voltage level translator between 1.8 V and 3.3 V respectively. TI recommends the use of a SN74AVC4T245. This is a quad (4-bit) dual supply translator suitable between needed 1.8 V and 3.3 V IO types. The SN74AVC4T245 is designed in a 3.5 mm × 4.0 mm package to minimize the form factor impact.

Additionally, the device VCNTL pins are open drain IOs, and require pull-up resistors to the 1.8 V rail (same rail as the device 1.8 V supply).

Figure 32 and Figure 33 illustrate the intended configuration inclusive of the UCD9244, SN74AVC4T245, and four DSPs – in the case where a reduced number of DSPs is required, the UCD9244 unused outputs can be configured as fixed rails or the alternate dual output UCD9244 can be substituted. Depending on the configuration and use case, the outputs of the UCD7242 can be tied together (requiring separate inductors) to increase the overall available supply current.

**Figure 32 VCNTL Level Translation (Example 1)**

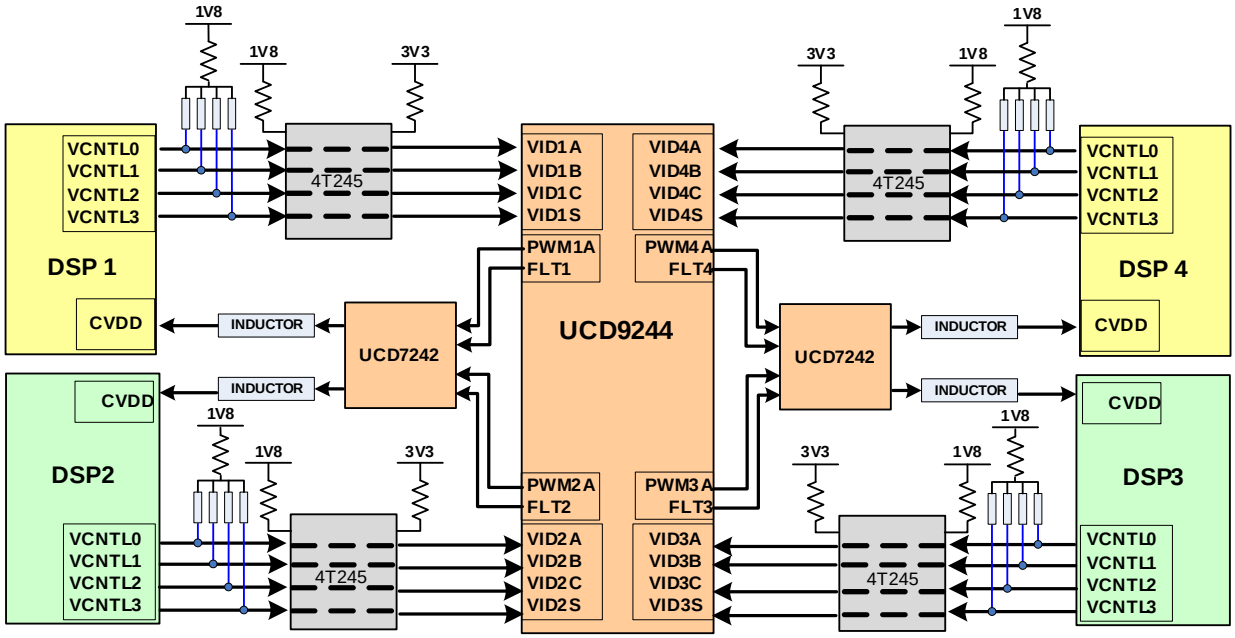
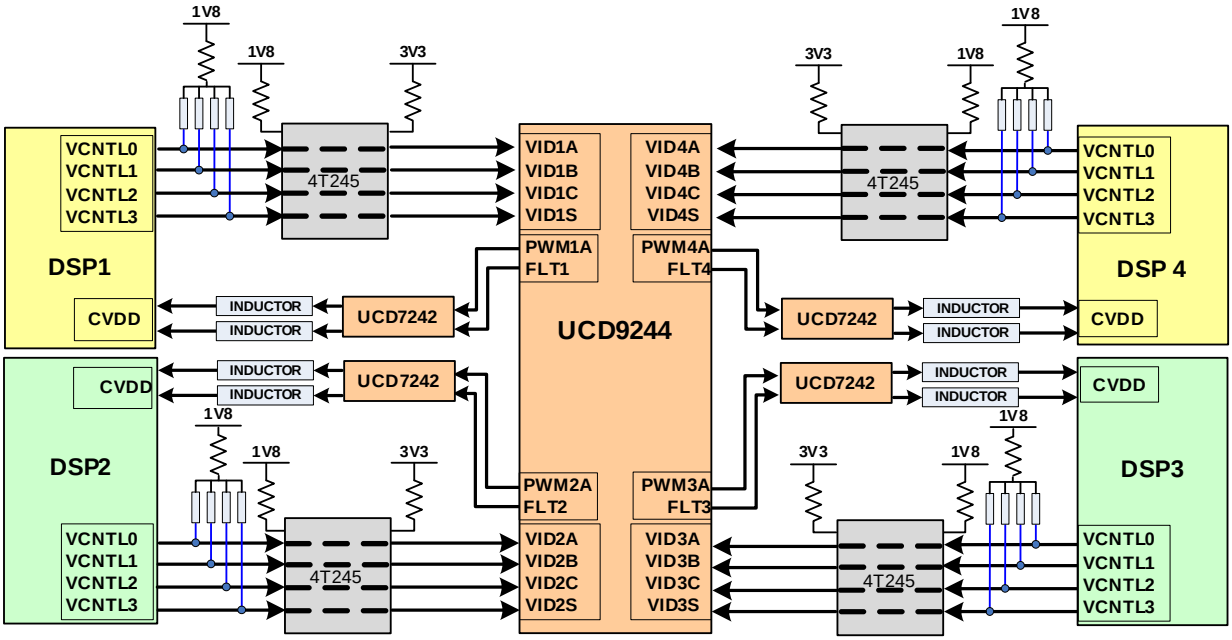


**Figure 33 VCNTL Level Translation (Example 2)**




### 5.9.2 VCNTL Connections

The SmartReflex interface between the device and recommended UCD9xxx power supply controller must be connected correctly to assure proper functionality. The UCD9244/22 power supply controllers support four and two SmartReflex enabled C66x devices respectfully. Proper connection between the device VCNTL or VID pins and either controller's VID interface is essential. The above figures properly illustrate the interconnectivity between controller and device.

### 5.9.3 SmartReflex Class Description

The SmartReflex class of operation is determined at run time, determination depends on power, topology, and current requirements of the end product specification.

Class-0: This class of operation accounts for a single value as determined during manufacturing tests, the fixed voltage is based on performance goals across all process corners. At the end of the manufacturing test the lowest acceptable voltage (while still meeting all performance requirements) is established and permanently programmed into each die. In this class of operation (Class 0) only the VCNTL or VID interface connections are used to program a fixed value of the external power source.

Class-3: This class of operation allows for continuous variability of the core voltage (scalable or variable). Voltage ranges are established during manufacturing test that identify the minimum and maximum voltage levels that still meet all performance requirements. In this class, an internal and dedicated processor module continuously determines the required voltage change and communicates this to the external power supply across the VCNTL or VID interface.

## 5.10 Power Saving Options

This section discusses handling of unused peripherals and other power-saving techniques.

### 5.10.1 Clock Gating Unused Peripherals

The C66x devices can be configured to place unused or inactive peripherals in a low-power state. Configuration of unused peripherals is covered in the C66x device data manual. After power-up, only those peripherals that are needed should be left enabled.

### 5.10.2 General Power Saving Techniques

This section identifies additional power saving techniques to be used if applicable.

- Where possible lower the clock frequencies, lower clock frequencies equates to lower power.
- The core and peripherals should be operated at the lowest frequency that meets the device and end product requirements.
- SerDes link power does not scale linearly with data rate. For SRIO and AIF, ports with higher link rates have a higher bandwidth/watt than slower links. Generally, running fewer high-speed links is less power than multiple slower links.
- Refer to the peripheral section of this application note for specific recommendations regarding unused peripherals and/or pins.

In addition to the above techniques, selecting the correct pull-up and pull-down resistor values can also reduce miscellaneous power. Use of alternate termination schemes such as a TPS511000 for the SDRAM Vtt termination source can reduce overall power consumption (depending on number of SDRAMs supported).

# 6 I/O Buffers

This section discusses buffer impedances, I/O timings, terminators, and signaling standards.

## 6.1 Process, Temperature, Voltage (PTV) Compensated Buffers

The impedance of I/O buffers is affected by process, temperature, and voltage. For the DDR3 interface, these impedance changes can impact performance and make it difficult to meet the JEDEC specifications. For this reason, the C66x device uses PTV compensated I/O buffers for the DDR3 interface. The PTV compensation works by adjusting internal impedances to nominal values based on an external referenced resistance. This is implemented by connecting a resistor between the PTV pin and $V_{SS}$. The PTV resistor must be a1% tolerance 45.3 Ω SMT resistor and connected between the pin and Vss (ground) as traces no longer than 0.5mm. (Texas Instruments is evaluating the acceptability of a 45 Ω PTV resistor and will update the respective documentation when testing is complete). For details, refer to the device data manual and the *DDR3 Design Guide for KeyStone Devices* (SPRABI1).

## 6.2 I/O Timings

The I/O timings in the KeyStone I data manual are provided for and based on the tester test load. These timings need to be adjusted based on the actual board topologies. It is highly recommended that timing for all high speed interfaces (including the high performance SerDes interfaces) on the KeyStone I design be checked using IBIS simulations (at a minimum). Simulating the high performance interfaces (SerDes) will require IBIS 5.0 AMI compliant models. IBIS models and parasitics incorporated in the IBIS models are based on IBIS loads and not the tester load.

## 6.3 External Terminators

Series impedance is not always needed but is useful for some interfaces to avoid over-shoot/under-shoot problems. Check the recommendations in the peripherals sections and/or perform IBIS or Matlab® simulations on each interface.

## 6.4 Signaling Standards

This section discusses signaling standards for various interfaces.

### 6.4.1 1.8 V LVCMOS

All LVCMOS I/O (input and output or bidirectional) buffers are JEDEC compliant 1.8-V LVMOS I/Os as defined in JESD 8-5. Several types of LVCMOS buffers are used in C66x devices, depending mainly on whether an internal pull-up or pull-down resistor is implemented. There also are some differences in the drive strength and impedance for some I/Os. For details on different LVCMOS buffer types, see the KeyStone I Data Manual.

These internal pull-up and pull-down resistors can be can be considered a 100 µA current source (with an actual range of 45 µA to 170 µA). This equates to a nominal pull-up/pull-down resistor of 18k Ω (with a possible range of 10k Ω to 42k Ω) The 1.8 V LVCMOS interfaces are not 2.5 V or 3.3 V tolerant so connections to 2.5 V or 3.3 V CMOS logic require voltage translation. For input buffers at moderate frequencies, TI's LVC logic family can be operated at 1.8 V and is 3.3 V tolerant. For faster signaling, TI's

AUC family is optimized to operate at 1.8 V and is also 3.3 V tolerant. Good options for voltage translation for 1.8 V outputs that need to drive 2.5 V or higher inputs would be the CBTLV family (for a non-buffered solution) or the AVC family (for a buffered solution). Some useful TI application reports on voltage translation options are:

- Voltage Translation Between 3.3 V, 2.5 V, 1.8 V, and 1.5 V Logic Standards With the TI (*SN74*)AVCA164245 and (*SN74*)AVCB164245 Dual-Supply Bus-Translating Transceivers Application Report (SCEA030)
- Selecting the Right Level-Translation Solution Application Report (SCEA035)
- Voltage Level Translation Product Portfolio

### 6.4.2 1.5V SSTL

The KeyStone I DDR3 interface is compatible with the *JEDEC 79-3C DDR3 Specification* [11]. The I/O buffers are optimized for use with direct connections to up to eight DDR3 SDRAMs and can be configured to drive a DDR3 UDIMM module. The DDR3 SSTL interface does not require series terminations on data lines (end terminations may be required). The 1.5 V SSTL DDR3 interface also supports active ODT (on-die-terminations).

### 6.4.3 SerDes Interfaces

There are many SerDes peripherals on the KeyStone I family of devices. The SerDes interfaces available include (others may apply): HyperLink, SRIO, PCI, SGMII, and AIF. These serial interfaces all use 8b/10b encoded links and SerDes macros.

**Note—**Not all SerDes peripherals are available on all C66x devices. Refer to the data manual for specific details.

These interfaces use a clock recovery mechanism so that a separate clock is not needed. Each link is a serial stream with an embedded clock so there are no AC timings or drive strengths as found in the LVCMOS or SSTL interfaces.

There are several programmable settings for each SerDes interface that affect the electrical signaling. The most important of these are: transmitter output amplitude, transmitter de-emphasis, and receiver adaptive equalization. Recommendations for these settings for particular board topologies are provided in *SerDes Implementation Guidelines for KeyStone Devices* (SPRABC1). The SerDes interfaces use CML logic. Compatibility to LVDS signals is possible and is described in Section 8.

# 7 Peripherals Section

This section covers each of the C66x device peripherals/modules (not all included, refer to the specific data manual). This section is intended to be used in addition to the information provided in the C66x device data manual, the module guides and relevant peripheral application reports. The four types of documents should be used as follows:

- Data Manual: AC Timings, register offsets
- Module Guide: Functional Description, Programming Guide
- Applications Reports: System level issues
- This Chapter: Configuration, system level issues not covered in a separate application report

Each peripheral section includes recommendations on how to handle pins on interfaces that are disabled or for unused pins on interfaces that are enabled. Generally, if internal pull-up or pull-down resistors are included, the pins can be left floating. Any pin that is output only can always be floated. Normally, if internal pull-up and pull-down resistors are not included, pins can still be floated with no functional issues for the device. However, this normally causes additional leakage currents that can be eliminated if external pull-up or pull-down resistors are used. Inputs that are not floating have a leakage current of approximately 100 µA per pin. Leakage current is the same for a high- or low-input (either pull-up or pull-down resistors can be used). When the pins are floating, the leakage can be several milliamps per pin. Connections directly to power or ground can be used only if the pins can be assured to never be configured as outputs and the boundary scan is not run on those pins.

## 7.1 GPIO/Device Interrupts

Documentation for GPIO/Interrupts:

- KeyStone Architecture General Purpose Input/Output (GPIO) User Guide (SPRUGV1)
- KeyStone IBIS Model File (specific to device part number)
- Using IBIS Models for Timing Analysis (SPRA839)

### 7.1.1 Configuration of GPIO/Interrupts

All GPIOs pins are multiplexed with other functions, with several being used for device configuration strapping options. The strapping options are latched by $\overline{\text{POR}}$ going high. After $\overline{\text{POR}}$ is high the pins are available as GPIO pins. Note: All pins must be driven to a logical state during boot and through $\overline{\text{POR}}$ being released. The GPIO pins are read during a $\overline{\text{POR}}$ boot function and if required are available for various GPIO functionalities after a successful boot.

GPIOs are enabled at power-up and default to inputs.

All GPIOs can be used as interrupts and/or EDMA events to any of the cores.

### 7.1.2 System Implementation of GPIO/Interrupts

It is recommended that GPIOs used as outputs have a series resistance (22 or 33 Ω being typical values). The value (or need) for the series resistor can be determined by simulating with the IBIS models.

If you want to have a GPIO input default to a particular state (low or high), use an external resistor. A pull-up resistor value of 1k Ω is recommended to make sure that it over-rides the internal pull-down resistor present on some GPIOs. If this GPIO is also used as a strapping option, the default state needs to also be the desired boot strapping option. The RESETSTAT signal can be used to tri-state logic that drives a GPIO boot strapping state during the POR transition.

### 7.1.3 GPIO Strapping Requirements

Table 18 defines briefly the strapping requirements for one of the KeyStone I family devices (refer to data manual for specific pin numbers). Included is the pin-to-function correlation needed to properly configure the device.

**Table 18 GPIO Pin Strapping Configurations**

| | | | Primary Function | | Secondary Function | |
|---|---|---|---|---|---|---|
| **Pin** | **Name** | **Boot Mode** | **pull-up** | **Pull Dn** | | |
| AJ20 | GPIO00 | LENDIAN | Little Endian | Big Endian | GPIO (after $\overline{POR}$) | |
| AG18 | GPIO01 | BOOTMODE00 | Boot Device | Boot Device | GPIO (after $\overline{POR}$) | Refer to 2.5 for additional details |
| AD19 | GPIO02 | BOOTMODE01 | Boot Device | Boot Device | GPIO (after $\overline{POR}$) | Refer to 2.5 for additional details |
| AE19 | GPIO03 | BOOTMODE02 | Boot Device | Boot Device | GPIO (after $\overline{POR}$) | Refer to 2.5 for additional details |
| AF18 | GPIO04 | BOOTMODE03 | Device Cfg | Device Cfg | SR ID | Specific device configurations |
| AE18 | GPIO05 | BOOTMODE04 | Device Cfg | Device Cfg | SR ID | Specific device configurations |
| AG20 | GPIO06 | BOOTMODE05 | Device Cfg | Device Cfg | GPIO (after $\overline{POR}$) | Specific device configurations |
| AH19 | GPIO07 | BOOTMODE06 | Device Cfg | Device Cfg | GPIO (after $\overline{POR}$) | Specific device configurations |
| AJ19 | GPIO08 | BOOTMODE07 | Device Cfg | Device Cfg | GPIO (after $\overline{POR}$) | Specific device configurations |
| AE21 | GPIO09 | BOOTMODE08 | Device Cfg | Device Cfg | GPIO (after $\overline{POR}$) | Specific device configurations |
| AG19 | GPIO10 | BOOTMODE09 | Device Cfg | Device Cfg | GPIO (after $\overline{POR}$) | Specific device configurations |
| AD20 | GPIO11 | BOOTMODE10 | PLL Multiplier/I2C | PLL Multiplier/I2C | GPIO (after $\overline{POR}$) | Specific device configurations |
| AE20 | GPIO12 | BOOTMODE11 | PLL Multiplier/I2C | PLL Multiplier/I2C | GPIO (after $\overline{POR}$) | Specific device configurations |
| AF21 | GPIO13 | BOOTMODE12 | PLL Multiplier/I2C | PLL Multiplier/I2C | GPIO (after $\overline{POR}$) | Specific device configurations |
| AH20 | GPIO14 | PCIESSMODE0 | Endpt/RootComplex | Endpt/RootComplex | GPIO (after $\overline{POR}$) | Specific device configurations |
| AD21 | GPIO15 | PCIESSMODE1 | Endpt/RootComplex | Endpt/RootComplex | GPIO (after $\overline{POR}$) | Specific device configurations |
| **End of Table 18** | | | | | | |

**Note—**Refer to the Boot and Configuration Specification in addition to the data manual for additional details.

### 7.1.4 Unused GPIO Pin Requirement

All GPIO serve multiple functions, each of the GPIO pins are required to be pulled to a logical state during boot (as defined by the boot method and as listed in the Bootloader Specification). After boot is complete ($\overline{POR}$ is deasserted), each GPIO pin is released and made available to the user as a general purpose IO. Each GPIO pin (after boot is complete) defaults to its identified state (refer to the data manual for default pull-up and pull-down conditions) unless otherwise configured. All application hardware must incorporate an appropriate design to permit flexibility between device configuration/boot and functional GPIO requirements.

If an external resistor is used to obtain a specific post boot state for any GPIO pin, an external 1k Ω - 4.7k Ω resistor to the appropriate rail is recommended.

**Note—**If any of the GPIO pins are attached to a trace, test point, another device, or something other than a typical no connect scenario, a pull-up or pull-down resistor is mandatory. The default internal pull-up resistor (only for GPIO00) and the default internal pull-down resistors (GPIO01 – GPIO15) are only suitable if nothing is connected to the pin.

## 7.2 HyperLink Bus

Documentation for HyperLink:

- Hyperlink for KeyStone Devices User Guide (SPRUGW8)
- C66x CPU and Instruction Set Reference Guide (SPRUGH7)
- KeyStone IBIS Model File (specific to device part number)

### 7.2.1 Configuration of HyperLink

The HyperLink interface is a high-performance TI developed interface intended for high speed data communication. Refer to the HyperLink Users Guide for additional configuration details.

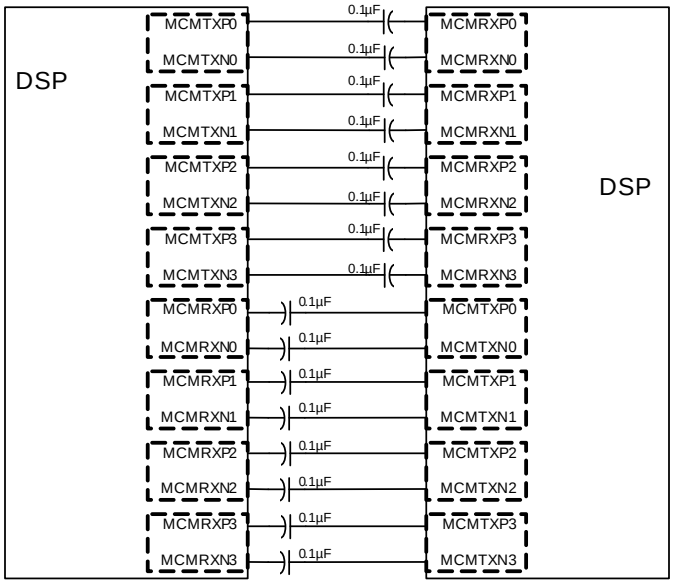
### 7.2.2 System Implementation of HyperLink Interface

Refer to Section 4.3.4 for details, guidelines, and routing requirements. This bus is intended to be a DSP-to-DSP interconnection bus.

### 7.2.3 HyperLink-to-HyperLink Connection

The Hyperlink interface bus is intended to be a short reach high-performance bus supporting a total of four interconnecting lanes between two DSPs operating at up to 12.5 GHz per lane (other configurations may exist).

**Figure 34 HyperLink Bus DSP-to-DSP Connection**



### 7.2.4 Unused HyperLink Pin Requirement

All Hyperlink clock and data pins (*MCMRXFLCLK, MCMRXFLDAT, MCMTXFLCLK, MCMTXFLDAT, MCMRXPMCLK, MCMRXPMDAT, MCMTXPMCLK, MCMTXPMDAT*) can be left floating when the entire Hyperlink peripheral is not used. Each unused Hyperlink clock and data pin will be pulled low when not in use through internal pull-down resistors.

In the event a partial number of lanes are used (two lanes instead of four), all clock and data pins must be connected. Unused lanes (both transmit and receive) can be left floating.

If the Hyperlink interface is not being used, the peripheral should be disabled in the MMR.

If the Hyperlink interface is not required, the Hyperlink regulator power pin (VDDR1_MCM) must still be connected to the correct supply rail with the appropriate decoupling capacitance applied. The EMI/Noise filter is not required when this interface is not utilized.

If unused, the primary Hyperlink clock input must be configured as indicated in Section 3.2.1, Figure 5. Pull-up must be to the CVDD core supply.

## 7.3 Inter-Integrated Circuit (I²C)

Documentation for I²C:

- Inter-Integrated Circuit (I2C) for KeyStone Devices User Guide (SPRUGV3)
- IBIS Model File for KeyStone Devices (specific to device part number)
- Using IBIS Models for Timing Analysis (SPRA839)
- Philip's I²C Specification, Version 2.1

### 7.3.1 Configuration of I²C

The I²C peripheral powers up enabled. The input clock for the I2C module is SYSCLK. The I²C clock is further divided down using an internal PLL. There is a prescaler in the I²C module that needs to be set up to reduce this frequency. Refer to the Bootloader and IRC users guide for additional information and details.

If the I²C signals are not used, the SDA and SCL pins can be left floating. This causes a slight increase in power due to leakage, which can be avoided by having pull-up resistors.

### 7.3.2 System Implementation of I²C

External pull-up resistors to 1.8 V are needed on the device I2C signals (SCL, SDA). The recommended pull-up resistor value is 4.7k Ω.

Multiple I2C devices can be connected to the interface, but the speed may need to be reduced (400 kHz is the maximum) if many devices are connected.

The I2C pins are not 2.5 V or 3.3 V tolerant. For connection to 2.5 V or 3.3 V I2C peripherals, the *PCA9306 Dual Bidirectional I2C Bus and SMBus Voltage-Level Translator Data Sheet* (SCPS113) can be used. Section 7.3.3 describes in greater detail the interconnection.

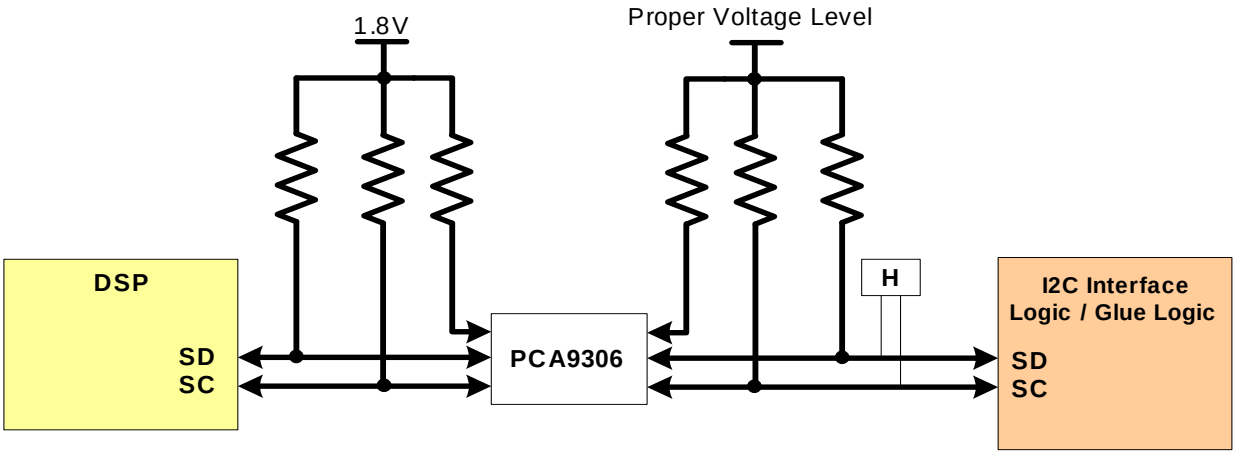
### 7.3.3 I²C Interface

The I²C pins of the device are not 2.5 or 3.3 V compatible, therefore it is necessary that any interconnection between the device's I²C pins and external logic be connected using a voltage level translator between 1.8 V pins and external logic. TI recommends the use of a PCA9306. This is a dual (2-bit) dual supply translator suitable between needed 1.8 V and external logic IO types. The PCA9306 is designed in a small 3.0 mm × 2.0 mm package to allow for ease of placement.

Additionally, the device I²C pins are open drain IOs, and require pull-up resistors to the 1.8 V rail (same rail as the device 1.8 V supply).

Figure 35 illustrates the intended configuration inclusive of the PCA9306, DSP, and as an example a EEPROM. This configuration illustrates the connection topology for a single DSP, in the case where multiple DSPs are used; each I2C interface must include the same configuration.

**Figure 35 I2C Voltage Level Translation**




### 7.3.4 Unused I2C Pin Requirement

All I²C clock and data pins (*SCL and SDA*) can be left floating when the I²C interface is not used. The unused I²C clock and data pins will be tri-stated when not in use.

## 7.4 Ethernet

Documentation for EMAC:

- KeyStone Architecture Gigabit Ethernet (GbE) Switch Subsystem User Guide (SPRUGV9)
- SGMII Specification (ENG-46158), Version 1.8, dated April 27, 2005 [7]
- SerDes Implementation Guidelines for KeyStone Devices (SPRABC1)

### 7.4.1 Configuration of EMAC, SGMII and MDIO

The EMAC interface is compliant with the *SGMII Specification (ENG-46158)*, Version 1.8 that specifies LVDS signals. Only the data channels are implemented so that the connected device must support clock recovery and not require a separate clock signal. When EMAC is enabled, the MDIO interface is enabled.

The MDIO interface (MDCLK, MDIO) uses 1.8 V LVCMOS buffers. EMAC must be enabled via software before it can be accessed unless the Boot over Ethernet boot mode is selected.

If EMAC is used, a RIOSGMIICLKP/N clock must be provided and the SerDes must be set up to generate a 1.25 Gbps link. The PLL multiplier settings for the three recommended RIOSGMIICLKP/N clocks frequencies are given in Table 19. Although the SGMII SerDes share a reference clock with the SRIO SerDes, they have separate PLLs which can be set up with different multipliers.

**Table 19 SGMII PLL Multiplier Settings**

| Reference Clock MHz | PLL Multiplier | Full Rate (Gpbs) | Half Rate (Gpbs) | Quarter Rate Gpbs) |
|---|---|---|---|---|
| 156.25 | 8 | 2.50 | 1.25 | N/A |
| 156.25 | 10 | 3.125 | N/A | N/A |
| 250.00 | 5 | 2.50 | 1.25 | N/A |
| 312.50 | 4 | 2.50 | 1.25 | N/A |
| 312.50 | 5 | 3.125 | N/A | N/A |

Refer to the data manual, users guide, and application notes for a full listing of rates supported.

If EMAC is not used, the SerDes signals can be left unconnected. MDIO can be left unconnected, but results in an increase in leakage current. This could be avoided by adding an external pull-up resistor. If both EMAC and SRIO are not used, the RIOSGMIICLKP/N pins should be terminated as shown in Figure 5. See Section 7.4.4 for additional detail.

### 7.4.2 System Implementation of SGMII

SGMII utilizes LVDS signaling. The C66x device uses a CML based SerDes interface that requires AC coupling to interface to LVDS levels; Texas Instruments recommends the use of a 0.1 µF AC coupling capacitors for this purpose. The SerDes receiver includes a 100 Ω internal termination so an external 100 Ω termination is not needed. Examples of SerDes to LVDS connections are given in the following sections.

If the connected SGMII device does not provide common-mode biasing, external components need to be added to bias the LVDS side of the AC-coupling capacitors to the nominal LVDS offset voltage, normally 1.2 V. Additional details regarding biasing can be found in the application note *Clocking Design Guide for KeyStone Devices (SPRABI4)*.

The SGMII interface supports hot-swap, where the AC coupled inputs of the device can be driven without a supply voltage applied.

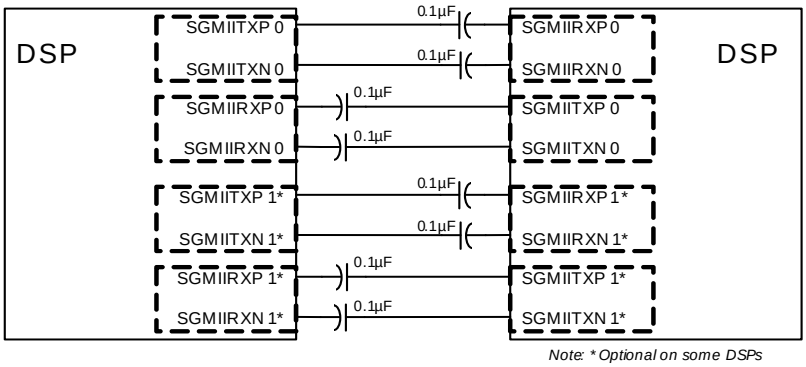
SRIO/SGMII SerDes power planes and power filtering requirements are covered in Section 6.3.

### 7.4.3 SGMII MAC to MAC Connection

The SGMII interface can be connected from the C66x device to the PHY or from the C66x device to a MAC, including KeyStone-to-KeyStone device direct connects. An example of the hardware connections is shown in Figure 36. For auto-negotiation purposes, the KeyStone I device can be configured as a master or a slave or it can be set up for fixed configuration. If the KeyStone I device is connected to another MAC, the electrical compatibility must be evaluated to determine if additional terminations are needed.

**Note—**Not all devices contain the implementation shown. Your specific C66x device should be properly configured for the correct number of SGMII interfaces shown in the data manual.

**Figure 36 SGMII MAC to MAC Connection**




### 7.4.4 Unused SGMII Pin Requirement

All unused SGMII pins must be left floating. As an additional note, should the SGMII interface not be required; the peripherals should be disabled. In the event only one of the two SGMII interfaces is required, the unused SGMII interface must be disabled through the MMR of the device.

The SGMII shares a common input clock with the SRIO interface, if either of these interfaces is used; the respective power must still be properly connected in accordance with this specification. Additionally, if the SGMII interface is used, the appropriate amount of decoupling/bulk capacitance must be included.

If the both of the SGMII interfaces are not used, the SGMII regulator power pin (VDDR3_SGMII) must still be connected to the correct supply rail with the appropriate decoupling capacitance applied. The EMI/Noise filter is not required when this interface is not utilized.

If both SRIO and SGMII are unused, the primary SRIOSGMIICLK clock input must be configured as indicated in Section 3.2.1, Figure 5. Pull-up must be to CVDD core supply. (Note: *both interfaces must be unused in order to pull-up the unused clock signal.*)

## 7.5 Serial RapidIO (SRIO)

Relevant documentation for SRIO:

- Serial RapidIO (SRIO) for KeyStone Devices User Guide (SPRUGW1)

- RapidIO Interconnect Part VI: Physical Layer 1×/4× LP-Serial Specification, Version 2.0.1 [10]
- SerDes Implementation Guidelines for KeyStone Devices (SPRABC1)

### 7.5.1 Configuration of SRIO

SRIO defaults disabled and with internal memories for the module in a sleep state. The memories, followed by the module, must be enabled by software before use (unless Boot over SRIO is selected). There are two SRIO lanes. A simple form of SRIO forwarding is supported to allow a daisy chain implementation.

The SRIO requires a differential reference clock: RIOSGMIICLKP/N. Supported frequencies for this clock are 125 MHz, 156.25 MHz, and 312.5 MHz. The SerDes used in the SRIO solution has a PLL that needs to be configured based on this reference clock and the desired link rate. Link rates can be full, half or quarter rate relative to the PLL frequency. Refer to Table 20 for PLL multiplier settings relative to link rate.

**Table 20 SRIO PLL Multiplier Settings**

| Reference Clock | PLL Multiplier | Full Rate | Half Rate | Quarter Rate | Eight Rate |
|---|---|---|---|---|---|
| (MHz) | | (Gbps) | (Gbps) | (Gbps) | (Gbps) |
| 312.50 | 8 | N/A | 5.000 | 2.500 | 1.250 |
| 312.50 | 5 | 6.250 | 3.125 | N/A | N/A |
| 156.25 | 20 | 3.125 | 1.5625 | N/A | N/A |
| 156.25 | 16 | N/A | N/A | 2.500 | 1.250 |
| 156.25 | 10 | 6.250 | 3.125 | N/A | N/A |
| 125.00 | 25 | N/A | 6.250 | 3.125 | N/A |
| 125.00 | 20 | N/A | 5.000 | 2.500 | 1.250 |
| 125.00 | 12.5 | N/A | 3.125 | N/A | N/A |
| **End of Table 20** | | | | | |

It is possible to configure the C66x device to boot load application code over the SRIO interface. Boot over SRIO is a feature that is selected using boot strapping options. For details on boot strapping options, see the KeyStone I data manual.

If the SRIO peripheral is not used, the SRIO link pins can be left floating and the SerDes links should be left in the disabled state.

The SRIO SerDes ports support hot-swap, where the AC coupled inputs of the device can be driven without a supply voltage applied.

If the SRIO peripheral is enabled but only one link is used, the pins of the unused link can be left floating.

### 7.5.2 System Implementation of SRIO

The Serial RapidIO implementation is compliant to the *RapidIO Interconnect Part VI: Physical Layer 1×/4× LP-Serial Specification*, Version 2.0.1.

For information regarding supported topologies and layout guidelines, see *SerDes Implementation Guidelines for KeyStone Devices* (SPRABC1).

Suggestions on SRIO reference clocking solutions can be found in Section 3.4.

SRIO/SGMII SerDes power planes and power filtering requirements are covered in Section 5.

### 7.5.3 Unused SRIO Pin Requirement

All unused SRIO lanes must be left floating and the unused lanes properly disabled through the MMR. If the entire SRIO interface is not required, the SRIO peripheral should be disabled.

The SRIO shares a common input clock with the SGMII interface. If either of these interfaces are used the respective power is still required to be connected in accordance with this specification and the appropriate decoupling/bulk capacitance included.

If the SRIO interface is not required, the SRIO regulator power pin (VDDR4_SRIO) must still be connected to the correct supply rail with the appropriate decoupling capacitance applied. The EMI/Noise filter is not required when this interface is not utilized.

If both SRIO or SGMII are unused, the primary SRIOSGMIICLK clock input must be configured as indicated in Section 3.2.1, Figure 5. Pull-up must be to CVDD core supply.

**Note**—Both interfaces must be unused in order to pull-up the unused clock signal.

## 7.6 Peripheral Component Interconnect Express (PCIe)

Relevant documentation for SRIO:

- PCI Express (PCIe) for KeyStone Devices User Guide (SPRUGS6)
- PCI Express Base Specification, revision 1.0
- PCI Express Base Specification, Version 2.0.1
- OCP Specification, revision 2.2

### 7.6.1 PCIe Features Supported

PCI Express is a point-to-point serial signaling protocol incorporating two links (consisting of one TX and one RX differential pair each). Supported is a single ×2 configuration or a single ×1 configuration (2 separate ×1 links are not supported). TI's PCIe interface supports (depending upon the protocol version), either 2.5 Gbps or 5.0 Gbps data transfer in each direction (less 8b/10b encoding overhead).

The device PCIe interface supports a dual operating mode (either Root complex (RC) or end point (EP)).

### 7.6.2 Configuration of PCIe

The PCIe mode is controlled by pinstrapping the two MSB GPIO bits (GPIO14:15). Table 21 illustrates the mode configuration. Specific details and proper configuration of the PCIe (if used) is identified in detail in the PCIe Users Guide.

**Table 21 PCIe (GPIO) Configuration Table**

| | GPIO15 | GPIO14 | Selection |
|---|---|---|---|
| | PCIMODE1 | PCIMODE0 | |
| pull-up/Dwn | 0 | 0 | PCIe in End Point Mode |
| | 1 | 0 | PCIe in Legacy End Point Mode |
| | 0 | 1 | PCIe in Root Complex Mode |
| | 1 | 1 | NOT VALID – Do Not Use |

### 7.6.3 Unused PCIe Pin Requirement

All unused PCIe lanes must be left floating and the unused lanes properly configured in the MMR. If the entire PCIe interface is not required, the PCIe peripheral should be disabled in the MMR.

If the PCIe interface is not required, the PCIe regulator power pin (VDDR2_PCIe) must still be connected to the correct supply rail with the appropriate decoupling capacitance applied. The EMI/Noise filter is not required when this interface is not utilized.

If unused, the PCIe clock must be configured as indicated in Section 3.2.1, Figure 5. Pull-up must be to CVDD core supply.

## 7.7 Antenna Interface (AIF)

Relevant documentation for AIF:

- Antenna Interface 2 (AIF2) for KeyStone Devices User Guide (SPRUGV7)
- OBSAI Reference Point 4 Specification, Version 1.1 [1]
- OBSAI Reference Point 3 Specification, Version 4.1 [2]
- OBSAI Reference Point 2 Specification, Version 2.1 [3]
- OBSAI Reference Point 1 Specification, Version 2.1 [4]
- CPRI Specification, Version 4.1 [5]
- Electrical Specification (IEEE-802.3ae-2002), dated 2002 [9]

### 7.7.1 Configuration of AIF

AIF defaults disabled and with the internal memories for the module in a sleep state. The memories, followed by the module, must be enabled by software before use.

There are two protocol modes supported on the AIF interface: OBSAI and CPRI. The mode is selected by software after power-up. All links are the same mode.

The AIF module requires the AIF reference clock (SYSCLKP/N) to drive the SerDes PLLs and requires frame sync timing signals provided by the frame sync module. The frame sync clock provided to the FSM has the following requirements:

- RP1 mode:
  - RP1CLKP/N must be 30.72 MHz (8× UMTS chip rate)
  - RP1FBP/N must provide a UMTS frame boundary signal
- Non-RP1 mode:
  - RADSYNC must be between 1 mS and 10 mS
  - PHYSYNC must provide UMTS frame boundary pulse

For proper operation of the AIF, the SYSCLKP/N (which is the antenna interface SerDes reference clock) and the frame sync clock (either RP1CLKP/N or ALTFSYNCCLK) must be generated from the same clock source and must be assured not to drift relative to each other.

The AIF reference clock and the SerDes PLL multiplier are used to select the link rates. Both CPRI and OBSAI have 3 supported line rates that run at 2×, 4×, and 8× the base line rate. The SerDes line rates can be operated at half rate, quarter rate, or eighth rate of the PLL output. For that reason, it is suggested that the AIF SerDes PLL be run at the 8× line rate. Each link pair can be configured as half rate (8×), quarter rate (4×), or eighth rate (2×). Table 22 illustrates the possible clocking variations for the AIF SerDes.

If OBSAI 8× and 4× links are used, the device minimum frequency is 1 GHz. If an OBSAI 2× link is used, or if CPRI is used, the device minimum frequency is 800 MHz.

**Table 22 AIF SerDes Clocking Options**

| | Reference Clock (MHz) | PLL Multiplier | 8× (Gbps) | 4× (Gbps) | 2× (Gbps) |
|---|---|---|---|---|---|
| CPRI | 122.88 | 20 | 4.9152 | 2.4576 | 1.2288 |
| | 153.60 | 16 | 4.9152 | 2.4576 | 1.2288 |
| | 307.20 | 8 | 4.9152 | 2.4576 | 1.2288 |
| OBSAI | 122.88 | 25 | 6.250 | 3.072 | 1.536 |
| | 153.60 | 20 | 6.250 | 3.072 | 1.536 |
| | 307.20 | 10 | 6.250 | 3.072 | 1.536 |
| **End of Table 22** | | | | | |

The AIF SerDes ports support hot-swap, where the AC coupled inputs of the device can be driven without a supply voltage applied.

### 7.7.2 System Implementation of AIF

In OBSAI RP3 mode, the interface is electrically compatible with the *OBSAI RP3 Specification*, Version 4.1.

In CPRI mode, the interface is electrically compatible with the *XAUI Electrical Specification* (IEEE-802.3ae-2002).

For information regarding supported topologies and layout guidelines, see the *SerDes Implementation Guidelines for KeyStone Devices* (SPRABC1).

Suggestions on AIF reference clocking solutions can be found in Section 3. AIF SerDes power planes and power filtering requirements are covered in Section 5.

**Table 23 AIF2 Timer Module Configuration Options**

| RAD Timer Sync | PHYTimer Sync | RP1Timer Sync | RP1 Timer Clock | Intended Use |
|---|---|---|---|---|
| | | RP1FBP/N | RP1CLKP/N | RP1 or differential sync & clock |
| RADSYNC | PHYSYNC | | | Non-RP1 single ended sync |

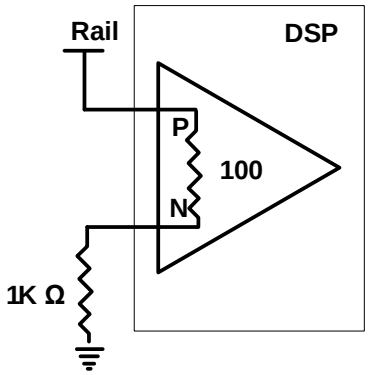
### 7.7.3 Unused AIF Pin Requirement

All unused AIF transmit and receive lanes must be left floating and the unused lanes properly disabled in the MMR. If the entire AIF interface is not required, the AIF peripheral should be disabled in the MMR and all link pins can be left floating. The reference clock should be terminated as shown in Figure 5.

If the AIF interface is not required, the AIF regulator power pins (VDDR5_AIF1 and VDDR6_AIF2) must still be connected to the correct supply rail with the appropriate decoupling capacitance applied. The EMI/Noise filters are not required when this interface is not utilized.

If the LVDS inputs (RP1CLKP/N pins Y28/AA28 and RP1FBP/N pins Y29/AA29) are not used, external connections should be provided to generate a valid logic level. The recommended connections for unused LVDS inputs are shown in Figure 37. The 1k Ω resistor is used to reduce power and be connected to the same 1V8 supply rail to which the IOs are connected.

**Figure 37 Unused LVDS Inputs**




### 7.7.4 System Implementation of RP1

For an RP1 compliant interface, the frame sync clock and frame sync burst signal defined by the RP1 Specification should be connected to RP1CLKP/N and RP1FBP/N, respectively.

LVDS 1:N buffers (such as the SN65LVDS108 or CDCL1810) can be used to connect these signals to multiple devices on a single board, however it is strongly recommended that the new high performance CDCM6208 low jitter, low power clock sources be used. The 100 Ω LVDS termination resistor is included in the C66x device LVDS receiver so an external 100 Ω resistor is not needed. These are standard LVDS inputs so, unlike the LJCB inputs, these inputs should not be AC coupled. They should be driven directly by an LVDS compliant driver.

The EXTFRAMEEVENT output is available to generate a frame sync output to other devices based on the frame clock and frame sync inputs. Its switching frequency and offset are programmable in the FSM. This output edge is not aligned with the frame clock input so take care if this output needs to be latched based on this clock.

For information on clocking distribution options for the single-ended frame sync clocks, see Section 4.2.

### 7.7.5 Unused RP1 Pin Requirement

If the RP1 interface is not used it is recommended that the RP1 clk input pins be connected in accordance with Figure 37. The EXTFRAMEEVENT output pin can be left floating. If the RP1 interface is not required, the RP1/AIF peripheral should be disabled in the MMR.

## 7.8 DDR3

Relevant documentation for DDR3:

- DDR3 Memory Controller for KeyStone Devices User Guide (SPRUGV8)
- DDR3 Design Guide for KeyStone Devices (SPRABI1)
- JEDEC JESD79-3C [11]

### 7.8.1 Configuration of DDR3

The DDR3 peripheral is enabled at power-up.

The DDR3 output clock is derived from the DDR3 PLL that uses DDRCLKP/N as a reference clock. The DDR3 PLL operates at 20× the DDRCLKP/N frequency and the DDR3 output clock is 1/2 of the PLL output clock. For example, a 66.667 MHz reference clock results in a 1,333 MHz PLL output and a DDR3 output clock of 667 MHz for DDR3-1333 support.

### 7.8.2 System Implementation of DDR3

For information regarding supported topologies and layout guidelines, see the *DDR3 Design Guide for KeyStone Devices* (SPRABI1).

Suggestions on DDR3 reference clocking solutions can be found in Section 3.

### 7.8.3 Slew Rate Control

The C66x device incorporates two pins necessary to control the DDR3 slew rate. There are four (4) possible slew rate combinations. The slew rate pins (DDRSLRATE1:0) must be pulled low or high at all times (they are not latched). Pulling both DDRSLRATE input pins low selects the fastest slew rate. If the DDRSLRATE pins are both pulled high, the resulting slew rate is the slowest. For normal full speed operation the DDRSLRATE pins should be pulled low. Table 24 illustrates the possible combinations when controlling the slew rate for the DDR3 interface.

**Table 24 Slew Rate Control**

| Setting | Speed | DDRSLRATE1 | DDRSLRATE0 |
|---|---|---|---|
| 00 | Fastest | pull-down | pull-down |
| 01 | Fast | pull-down | pull-up |
| 10 | Slow | pull-up | pull-down |
| 11 | Slowest | pull-up | pull-up |

**Note—**Refer to the DDR3 implementation guide for specific details. Slew rates denoted in the table are relative and are highly dependant upon topologies, component selection, and overall design implementation.

### 7.8.4 Unused DDR3 Pin Requirement

If the DDR3 peripheral is disabled, all interface signals (including reference clocks) can be left floating and the input buffers are powered down.

All unused DDR3 address pins must be left floating. All unused error correction pins must also be left floating. All remaining control lines must also be left floating when unused. Unused byte lanes must be properly disabled in the appropriate MMR.

If the DDR3 interface is not required, the DDR3 PLL supply (AVDDA2) must still be connected and the ferrite bead installed to minimize noise.

If unused, the primary DDR3 clock input must be configured as indicated in Section 3.2.1, Figure 5. Pull-up must be to CVDD core supply. The VREFSSTL pin must be connected to the VREF (0.75V) supply regardless of whether the DDR3 interface is used or not used.

## 7.9 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- Emulation and Trace Headers Technical Reference Manual (SPRU655) (but note differences defined below)
- Boundary Scan Test Specification (IEEE-1149.1)
- AC Coupled Net Test Specification (IEEE-1149.6
- Clocking Design Guide for KeyStone Devices (SPRABI4)

### 7.9.1 Configuration of JTAG/Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant to both IEEE-1149.1 and 1149.6 (for SerDes ports). Boundary scan can be used regardless of the device configuration.

As an emulation interface, the JTAG port can be used in various modes:

- Standard emulation: requires only five standard JTAG signals
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in this mode.
- Trace port: The trace port allows real-time dumping of certain internal data. The trace port uses the EMU[18:00] pins to output the trace data, however, the number of pins used is configurable.

Emulation can be used regardless of the device configuration.

For supported JTAG clocking rates (TCLK), refer to the specific C66x device data manual. The EMU[18:00] signals can operate up to 166 Mbps, depending on the quality of the board level design and implementation.

Any unused emulation port signals can be left floating.

**Note—**Not all C66x devices will contain the same number of emulation or trace pins. Refer to your applicable data manual for the number of available emulation pins provided.

### 7.9.2 System Implementation of JTAG / Emulation

For most system level implementation details, see the Emulation and Trace Headers Technical Reference Manual (SPRU655). However, there are a few differences for KeyStone I device implementation compared with this document:

- Although the document implies 3.3 V signaling, 1.8 V signaling is supported as long as the TVD source is 1.8 V.

For a single device connection where the trace feature is used, the standard non-buffered connections can be used along with the standard 14 pin connector. If the trace feature is used, which requires the 60-pin emulator connector, the five standard JTAG signals should be buffered and TCLK and RTCLK should be buffered separately. It is recommended to have the option for an AC parallel termination on TCLK since it is critical that the TCLK have a clean transition. EMU0 and EMU1 should not be buffered since these are used as bidirectional signals when used for HS-RTDX.

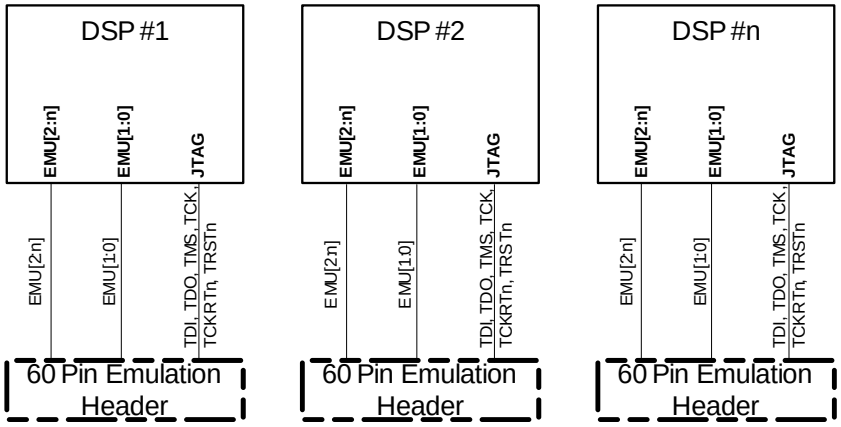
For a system with multiple DSPs that do not use the trace analysis features, the JTAG signals should be buffered as described above but the standard 14 pin connector can be used.

There are two recommended solutions if trace analysis is desired in a system with multiple DSPs.

Emulator with trace, solution #1: trace header for each DSP (see Figure 38):

- Pros
  - Most simple
  - Most *clean* solution electrically
- Cons
  - Expensive (multiple headers)
  - Takes up board real estate
  - No global breakpoints, synchronous run/halt

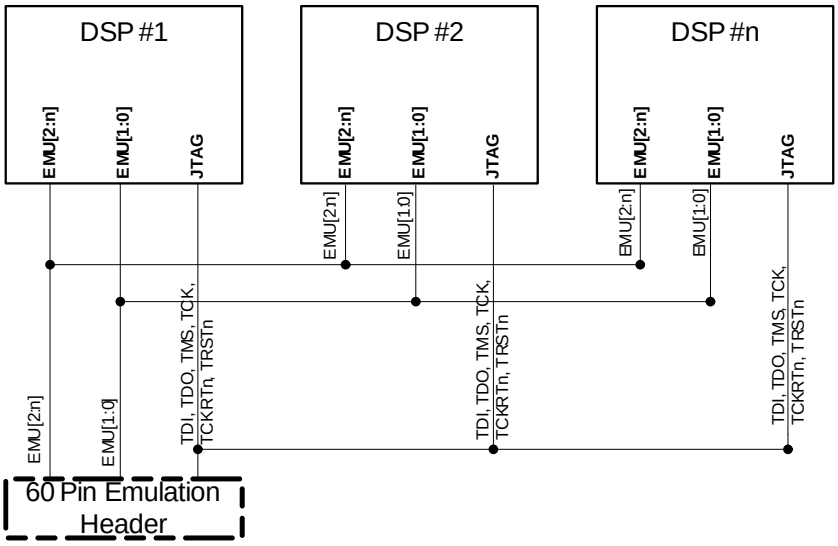
**Figure 38 Emulator with Trace Solution #1**



Emulator with trace, solution #2: single trace header (see Figure 39):

- Pros
  - Fairly *clean* solution electrically
  - Supports global breakpoints, synchronous run/halt
- Cons
  - Supports trace on only one device
  - Less bandwidth for trace (EMU0 used for global breakpoints)
  - Loss of AET action points on EMU1 (only significant if EMU1 has been used as a trigger input/output between devices. EMU0 can be used instead if needed).

**Figure 39 Emulator with Trace Solution #2**




No external pull-up/down resistors are needed since there are internal pull-up/down resistors on all emulation signals.

Although no buffer is shown, for multiple DSP connections it is recommended to buffer the five standard (TDI, TDO, TMS, TCK, and TRST) JTAG signals.

If trace is used, it is *not recommended* to add both a 60-pin header and a 14-pin header due to signal integrity concerns. 60-pin to 14-pin adapters are available to allow connection to emulators that only support the 14-pin connector (although 14-pin emulators do not support trace features).

Some emulators may not support 1.8 V I/O levels. Check emulators intended to operate with the C66x device to verify that they support the proper I/O levels. If 1.8 V levels are not supported, a voltage translator circuit is needed or a voltage converter board may be available. If the C66x device is in a JTAG chain with devices that have a different voltage level than 1.8 V (i.e., 3.3 V), voltage translation is needed.

Figure 40 illustrates a dual voltage JTAG solution using buffers to perform the voltage translation. The ALVC family for 3.3 V and the AUC family for 1.8 V are both used because they have similar propagation delays.

**Figure 40 Emulation Voltage Translation with Buffers**

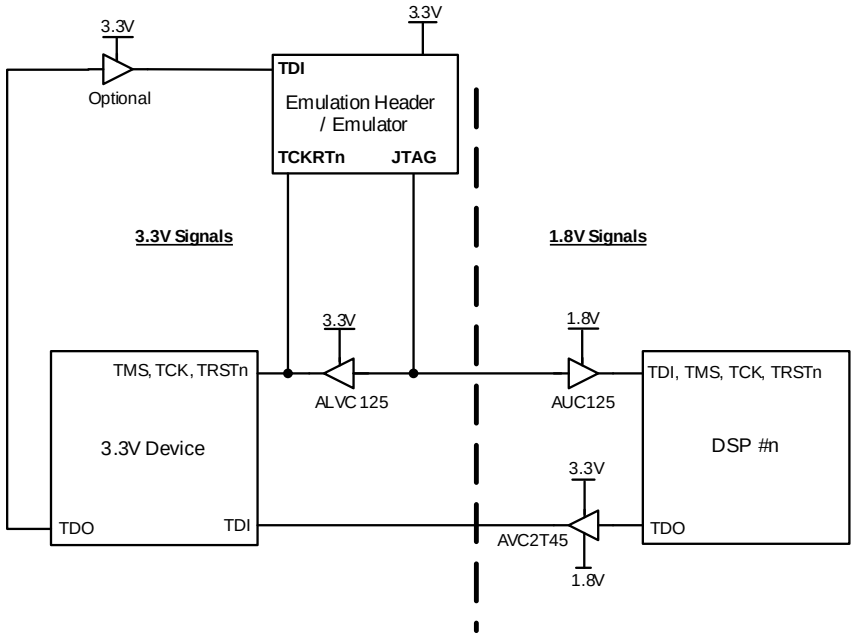
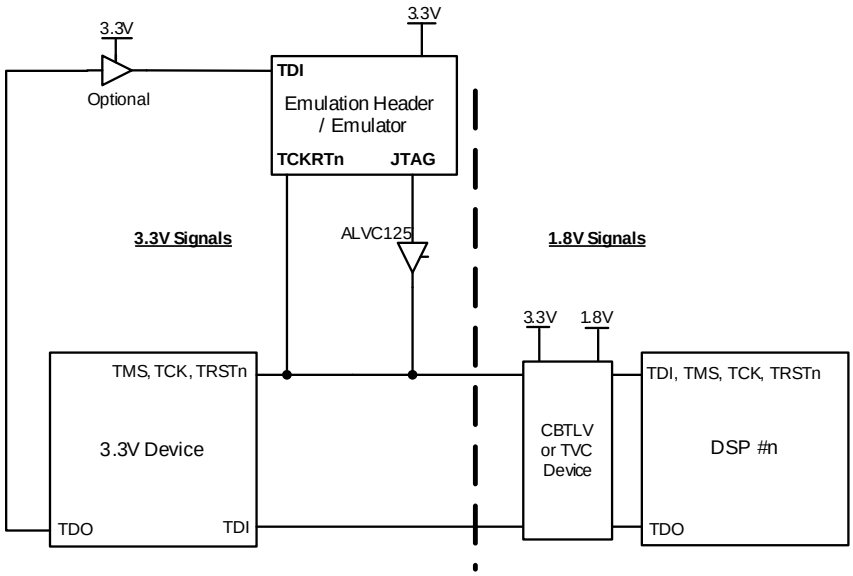



Figure 41 shows an example of using FET switch devices for voltage translation. If EMU0 and EMU1 are connected, use this approach since these are bidirectional signals.

**Figure 41 Emulator Voltage Translation with Switches**




If the trace signals are supported, they may need to have voltage translation as well. Due to the speed of the trace signals it is recommended that these signals be directly connected to the emulation header.

### 7.9.3 Unused Emulation Pin Requirement

The TI device contains both a JTAG and emulation pin interface. JTAG is a serial scan mechanism allowing for communication between a debugger and device. The emulation pins provide for a high performance output of select data captured from the device and transferred to an emulator and debugger.

If the JTAG and emulation interface is not used, all pins except $\overline{TRST}$ can be left floating. $\overline{TRST}$ must be pulled low to ground through a 4.7 K Ω resister (1K Ω resistor is preferred).

Refer to the data manual and emulation documentation for additional connectivity requirements.

## 7.10 UART

Relevant documentation for the UART:

- Universal Asynchronous Receiver/Transmitter (UART) for KeyStone Devices User Guide (SPRUGP1)
- C66x DSP CPU and Instruction Set Reference Guide (SPRUGH7)
- C66x CorePac User Guide (SPRUGW0)

The UART peripheral performs serial-to-parallel conversion to data received from a peripheral device connecting to the DSP and parallel-to-serial data conversion to data connecting between the DSP and peripheral device.

Figure 42 illustrates the concept of peripheral to DSP connection with autoflow control support (required on both connections)

**Figure 42 UART Connections with Autoflow Support**

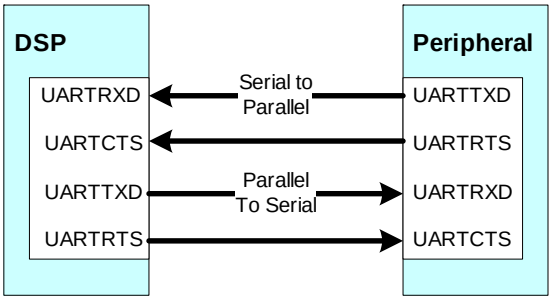
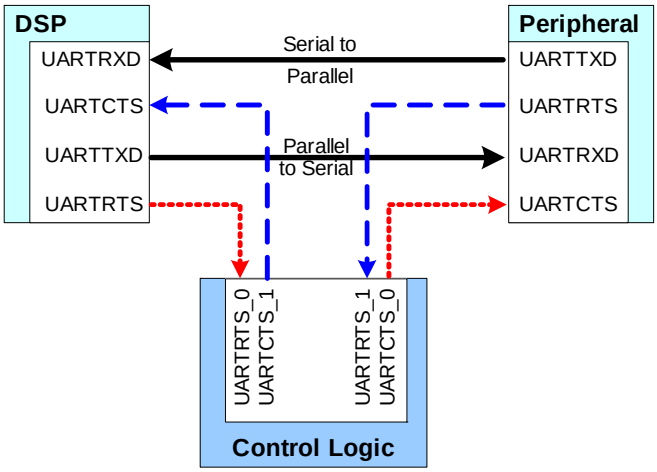


Figure 43 illustrates the concept of peripheral to DSP connection without support for autoflow control support.

**Figure 43 UART Connections without Autoflow Support**




### 7.10.1 Configuration of the UART

The UART peripheral is based on the industry standard TL16C550 asynchronous communications element, which is a functional upgrade of the TL16C450. Key configuration details are described in the Universal Asynchronous Receiver/Transmitter (UART) for KeyStone Devices User's Guide (SPRUGP1).

At a minimum the following must be configured:

| | |
|---|---|
| Receiver Buffer Register | Transmitter Holding Register |
| Interrupt Enable Register | Interrupt Identification Register |
| FIFO Control Register | Line Control Register |
| Divisor LSB Latch | Mode Definition Register |

### 7.10.2 System Implementation of the UART

The UART interface is intended to operate at 1.8 Vdc. Connection between the device UART interface and peripheral must be at a 1.8 V level to assure functionality and avoid damage to either the peripheral or device.

### 7.10.3 Unused UART Pin Requirements

The UART interface to the device contains four pins (CTS, RTS, TXD, and RXD). These pins (defined with respect to the device) are LVCMOS which when not used should be connected in the following manner:

| | | | |
|---|---|---|---|
| RTS (Request to Send) | Output | Leave Floating | (PD*) |
| CTS (Clear to Send) | Input | Leave Floating | (PD*) |
| TXD (Serial Data Transmit) | Output | Leave Floating | (PD*) |
| RXD (Serial Data Receive) | Input | Leave Floating | (PD*) |

**Note—***: The above recommendations are based on the peripheral being unused and no traces attached. If traces are attached to any of the peripheral pins the added pull-up (to DVDD18) or pull-down (to VSS) resistor the appropriate rail are needed.

Refer to the data manual and UART users guide for additional connectivity requirements.

## 7.11 Serial Port Interface (SPI)

Relevant documentation for the SPI Interface:

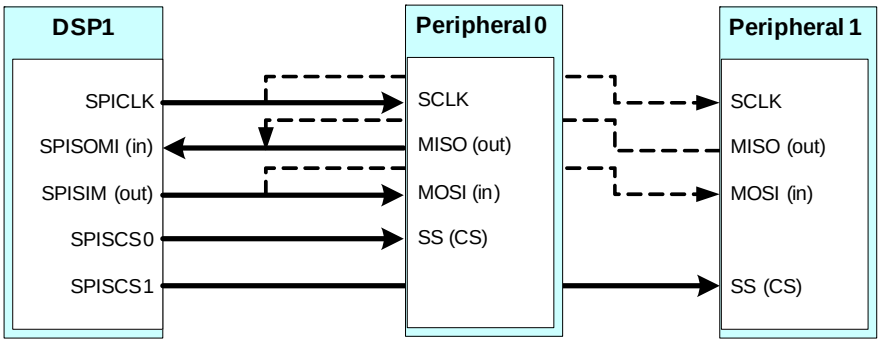
- Serial Peripheral Interface (SPI) for KeyStone Devices User Guide (SPRUGP2)
- C66x CPU and Instruction Set Reference Guide (SPRUGH7)
- C66x CorePac User Guide (SPRUGW0)

The SPI peripheral is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The device SPI interface can support multiple SPI slave devices (varies by device type and select/enable pins). The device SPI interface can operate as a master device only.

The SPI is normally used for communication between the device and common external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EEPROMs, and analog-to-digital converters.

The DSP must only be connected to SPI-compliant slave devices. Figure 44 illustrates the concept of DSP to two peripherals.

**Figure 44 SPI Connections**



### 7.11.1 Configuration of the SPI

The SPI peripheral is required to be configured correctly prior to use for a proper bit stream transfer.

### 7.11.2 System Implementation of the SPI

The SPI interface is intended to operate at 1.8 Vdc. Connection between the device SPI interface and peripheral must be at a 1.8 V level to assure functionality and avoid damage to either the peripheral or device.

Two key controls are necessary in order for the SPI to function: a) chip select control (SPISCS1:0), and b) Clock polarity and phase.

Refer to the SPI implementation and Users Guide for specific and detailed configuration.

### 7.11.3 Unused SPI Pin Requirements

The SPI interface to the device contains 5 pins (SPISCS0, SPICS1, SPICLK, SPISOMI, and SPISIMO). These pins (defined with respect to the device) are 1.8 V LVCMOS which when not used should be connected in the following manner:

| | | | |
|---|---|---|---|
| SPISCS0 (Chip Select 0) | Output | Leave Floating | (PU)* |
| SPISCS0 (Chip Select 1) | Output | Leave Floating | (PU)* |
| SPICLK (Master Clock) | Output | Leave Floating | (PD)* |
| SPISIMO (Serial Data Out) | Output | Leave Floating | (PD)* |
| SPISOMI (Serial Data In) | Input | Leave Floating | (PD)* |

**Note—***: The above recommendations are based on the peripheral being unused and no traces attached. If traces are attached to any of the peripheral pins the added pull-up (to DVDD18) or pull-down (to VSS) resistor to the appropriate rail are needed.

Refer to the data manual and SPI users guide for additional connectivity requirements.

## 7.12 External Memory Interface 16 (EMIF16)

Documentation for EMIF16:

- External Memory Interface (EMIF16) for KeyStone Devices (SPRUGZ3)
- KeyStone Architecture Bootloader User Guide (SPRUGY5)
- BSDL Model for your device
- IBIS Model File for your device
- Using IBIS Modes for Timing Analysis (SPRA839)

### 7.12.1 Configuration of EMIF16

The EMIF16 peripheral can be disabled using boot strapping options, as defined in the KeyStone I Data Manual and the C66x Bootloader User Guide. If the EMIF16 is enabled via boot strapping, it still needs to be enabled via software after a reset.

The clock to be used for EMIF16 can either be supplied externally to the AECLKIN pin or can be generated internally from the device core clock. The internally generated clock is referred to as SYSCLK6. After a reset, SYSCLK6 is device core clock / 6. The SYSCLK6 divider can be changed via software register accesses to PLL1.

One of the boot modes provides for booting over the EMIF16. In this mode, after reset, the device immediately begins executing from the base address of CS2 in 16-bit asynchronous mode. This would support booting from simple asynchronous memories such as NOR FLASH.

### 7.12.2 System Implementation of EMIF16

Generally, series resistors should be used on the EMIF16 signals to reduce overshoot and undershoot. They are strongly recommended for any output signal used as a synchronous latch. Generally acceptable values are 10, 22 or 33 ohms. To determine the optimum value, simulations using the IBIS models should be performed to check for signal integrity and AC timings. Significant signal degradation can occur when multiple devices are connected on the EMIF16. Simulations are the best mechanism for determining the best physical topologies and the highest frequency obtainable with that topology.

### 7.12.3 Unused EMIF16 Pin Requirements

If the EMIF16 peripheral is not used, the EMIF16 inputs can be left unconnected. Internal pull-up and pull-down resistors are included on this interface so leakage will be minimal. If only a portion of the peripheral is used, control pins that are not used should be pulled to a valid state with an external resistor and data pins that are not used can be left floating.

## 7.13 Telecom Serial Interface Port (TSIP)

Documentation for TSIP:

- Telecom Serial Interface Port (TSIP) for KeyStone Devices User Guide (SPRUGY4)
- BSDL Model for your device
- IBIS Model File for your device
- Using IBIS Models for Timing Analysis (SPRA839)

### 7.13.1 TSIP Configuration

TSIP0 and TSIP1 are independent serial interface ports. Each one has two clock inputs, two frame sync inputs, eight serial data inputs, and eight serial data outputs. All interface timing is derived from the clock and frame sync inputs. Each TSIP module can be individually configured to operate at either 8.192 Mbps, 16.384 Mbps, or 32.768 Mbps. All eight lanes are used at 8.192 Mbps, only the first four lanes are used at 16.384 Mbps, and only the first two lanes are used when at 32.768 Mbps.

TSIP outputs are configurable to simplify multiplexing of TDM streams. Unused output timeslots can be configured to drive high, drive low or be high impedance. Low-speed links can use simple wire-OR multiplexing when unused timeslots are high impedance. Higher speed links can be combined with OR logic when unused timeslots are driven low or AND logic can combine output streams when unused timeslots are driven high.

### 7.13.2 TSIP System Implementation

Series resistors should be used on TSIP clock inputs that are edge sensitive. These resistors need to be placed near the signal source. This prevents glitches on the clock signal transitions that could potentially disrupt TSIP timing. Most implementations do not need series terminations on the other TSIP control and data lines as long as the traces are kept short and routed cleanly.

The maximum TSIP performance is achievable only when using point-to-point connections. Termination resistors are only rarely needed in this topology. In a bused architecture where several devices are connected to the same TSIP interface, the traces should be routed from device to device in a single, multi-drop route without branches. Then a single termination can be implemented at the end of the bus to reduce over-shoot and under-shoot which minimizes EMI and crosstalk. This need is even more likely whenever a TSIP bus passes through board-to-board connectors. To determine the optimum value, simulations using the IBIS models should be performed to validate signal integrity and AC timings.

Multiple devices can be connected to a common TSIP bus using TDM mode. The additional loads require a reduction in the operating frequency. Also, the specific routing topology becomes much more significant as additional devices are included. The way to determine the best topology and maximum operating frequency is by performing IBIS simulations.

### 7.13.3 Unused TSIP Pin Requirements

If any of the TSIP inputs are not used, they can be left floating since all TSIP pins have internal pull-down resistors.

# 8 Terminations

## 8.1 SerDes-LVDS Termination Options

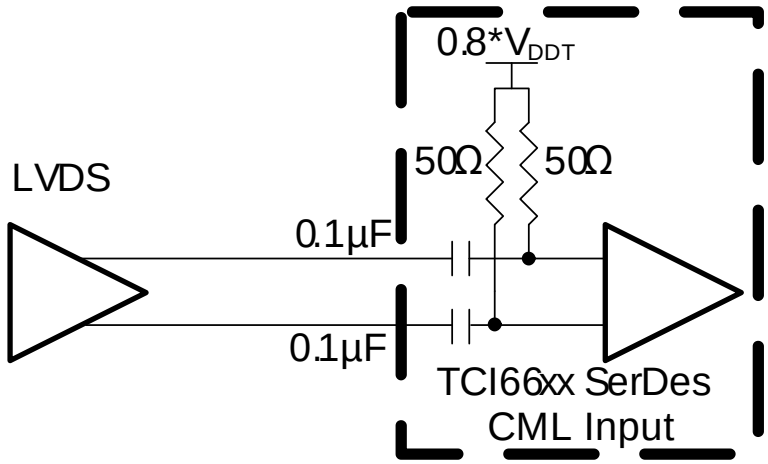
TI SerDes are CML implementations and do not directly support LVDS levels. Compatibility with standard LVDS signals is achievable with proper terminations as described in this section. Other termination options exist – each final selection must be modeled to determine the best solution for the intended end use application. Refer to this section and the application note "Clocking Design Guide for KeyStone Devices" for alternate solutions.

## 8.2 LVDS to CML Example

The following is an example of an LVDS to CML connection:

- Requires AC termination because the LVDS common-mode voltage is too high for the KeyStone I device SerDes receivers.
- CML receivers include 100 Ω termination needed by LVDS and include internal biasing (no external biasing needed).
- Refer to Figure 45.

**Figure 45 LVDS to CML Connection**

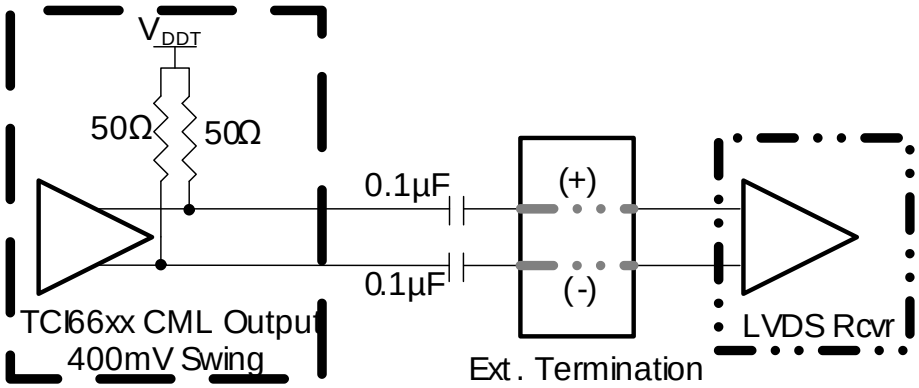



## 8.3 CML to LVDS Example

The following is an example of a CML to LVDS connection:

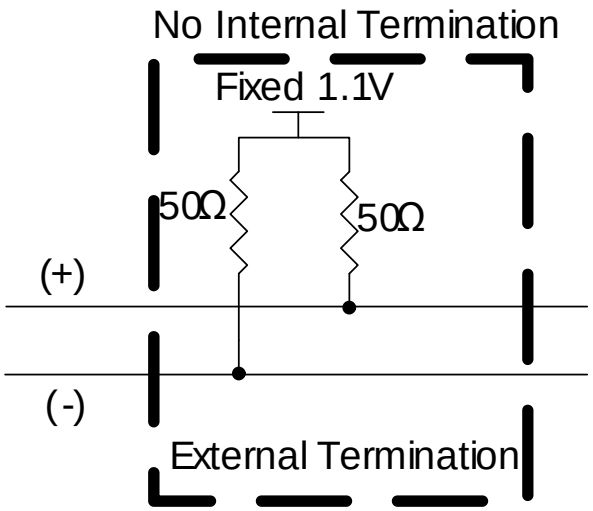
- Requires AC termination because C66x device CML output voltage is too low for LVDS receiver and the common-mode voltages are incompatible.
- LVDS receivers require 100 Ω terminations and proper biasing.
- Some LVDS receivers include 100 Ω termination and some do not.
- Some LVDS receivers include internal biasing and some do not.
- The basic connection diagram is shown in Figure 46.

**Figure 46 Basic CML to LVDS Connection Diagram**



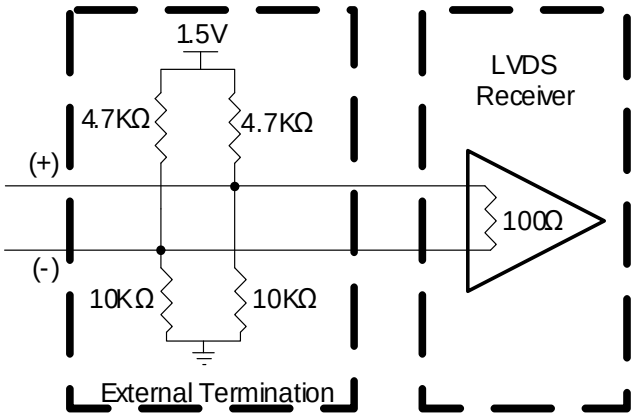

- If the LVDS receiver includes the 100 Ω termination and internal biasing, there is no need for external terminations
- If the LVDS receiver includes neither the100 Ωs or biasing, use the external terminations shown in Figure 47.

**Figure 47 External Terminations: Receiver Has No Internal Terminations**



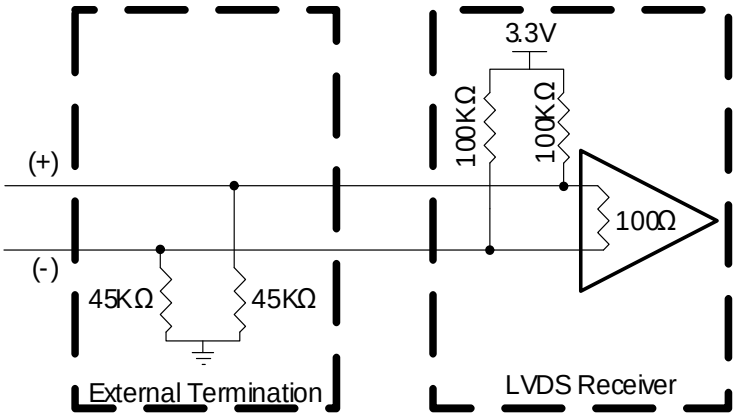

- If the LVDS receive includes the 100 Ω termination but no biasing, use the external terminations shown in Figure 48.

**Figure 48 Ext. Terminations: LVDS Receiver with 100 Ω**




If the LVDS receiver includes a 100 Ω termination and internal pull-up resistors (sometimes used for fail-safe), use the type of termination indicated in Figure 49. Adjust the external resistor values based on the $V_{cc}$ and internal resistors to generate a bias voltage of 1.0 to 1.2 V.

**Figure 49 External Terminations: Receiver with 100 Ω**




- There are other combinations that may be needed for other types of input buffers. The key factors to consider and design for are that there is a 100 Ω impedance and a bias voltage set around 1.2 V is required.

## 8.4 General Termination Details

The use of terminations in various nets is designed to address one of three major issues:

- signal overshoot
- signal undershoot
- fast slew rates

Depending on the nature of the signal, if an overshoot or undershoot were to occur, the resulting energy induced may be catastrophic to the interconnecting device (or DSP). Many standards – including SDRAM standards have overshoot and undershoot requirements that must be maintained in order to assure device reliability. The DSP and other devices also incorporate both source and sync current limitations as well as Vil/Vih & Vol/Voh requirements that must be maintained. Many of these established limitations are controlled by using terminations.

Clocking terminations many times require special consideration (AC or DC termination styles), in all cases proper positioning of the termination and selection of component is critical.

Terminations are also valuable tools when trying to manage reflections. Adding in a series termination on a particular net can relocate the point of reflection outside of the switching region (although this is better managed by physical placement).

It is always recommended that single-ended clock line, data, and control lines be modeled to establish the optimum location on the net.

To determine if a termination should be used (data, control, single-ended clock traces) the following test should be used:

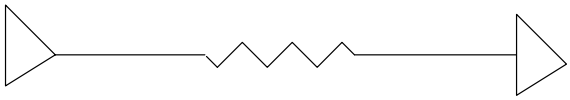
- If the uni-directional (one way) propagation delay for the trace(s) in question is ≤ 20% of the rise/fall time (whichever is fastest) or ≥ 80% of the rise/fall time (whichever is fastest) then a termination should not be needed.

Further determination of whether or not a termination is required can be ascertained using the second condition:

- A transmission line requires termination (to its intended impedance) if the uni-directional Tpd (propagation delay) for the respective net is ≥ 50% of the respective rise or fall time fall time (fastest of the two).

The most common of terminations are for single ended nets and follow the basic design illustrated in Figure 50:

**Figure 50 Basic Series Termination**



# 9 Power Saving Modes

The C66x device incorporates advanced power saving methods that can be utilized when power consumption is a concern. This includes disabling particular IOs to placing key peripherals into a hibernation state. The following section describes the low power methods and hibernation states to be used, the limitations and configuration methods.

Relevant documentation for Power Savings:

- KeyStone I Data Manual

The KeyStone I family of devices has been designed with four basic modes of operation:

- Off - Power off, no power supplied to the device at all
- Active - Power on, out of reset and fully functional
- Stand by - Power on, not in a fully active state, lower power then Active, greater power than hibernation modes
- Hibernation - Two specific operational modes intended to significantly reduce power consumption (includes level 1 & 2).

Refer to the following sections, the specific data manual, and respective application notes for additional details on configuration and application of different power saving and operational modes.

## 9.1 Standby Mode

The KeyStone I family of devices incorporates a standby mode. This mode of operation is intended to provide maximum readiness from the device. This mode differs from additional power saving modes identified in Section 9.2 in that standby mode does not incorporate all the advanced power savings features associated with other modes.

In actuality there exist many different combinations of standby mode – different combinations would take into account such interfaces as SRIO, Ethernet, PCIe, and HyperLink.

During standby mode – IO status is not impacted.

In a standby mode the status for each respective peripheral (if available) is indicated in Table 25. Refer to the specific device data manual for detailed descriptions on power saving modes.

**Table 25 Stand By Peripheral Status (Part 1 of 2)**

| Peripheral | Status | Notes |
|---|---|---|
| Debug Interface | ON | |
| PCIe | ON | |
| DDR3 | ON | |
| SRIO | ON | |
| AIF | ON | |
| Accelerator(s) | ON | Refer to data manual for applicable accelerators |
| HyperLink | ACTIVE | |
| FFTC | OFF | |
| Cores | INACTIVE | Refer to application note and data manual for core status during stand by mode |

**Table 25 Stand By Peripheral Status (Part 2 of 2)**

| Peripheral | Status | Notes |
|---|---|---|
| SGMII | ACTIVE | |
| EMIF | ACTIVE | |
| **End of Table 25** | | |

## 9.2 Hibernation Modes

The C66x device incorporates several power saving modes referred to as "Hibernation Modes." These modes are intended to conserve power during operation when only partial functionality is required (periods of inactivity). The benefits to utilizing a hibernation mode include faster wake up times (as compared to cold boot) in addition to the typical power savings obtained.

Access to the particular hibernation modes is obtained through writable registers – refer to the data manual for the memory map.

Each C66x device incorporates different hibernation modes; refer to the specific data manual and application notes for additional details.

There exist multiple hibernation modes for the KeyStone I family devices; they are described briefly below.

### 9.2.1 Hibernation Mode 1

During hibernation mode 1, only the MSMC SRAM memory content is retained. The MSMC MMR is not retained when placed in hibernation mode 1. Prior to entering this specific hibernation mode the bootcfg MMR PWRSTATECTL must be properly configured and set (refer to the appropriate users guide for configuration on entering and exiting this hibernation mode).

This hibernation mode does require a chip level reset to exit, which is initiated using an external reset pin. The estimated wake-up time from this hibernation mode is less than 100 mS.

### 9.2.2 Hibernation Mode 2

During hibernation mode 2, the MSMC SRAM memory contents are lost and only information stored in the DDR3 SDRAM is retained. The MSMC MMR is not retained when placed in hibernation mode 2. After a chip level reset is asserted, the MSMC is reset to its default condition (settings).

This hibernation mode does require a chip level reset to exit, which is initiated using an external reset pin. The estimated wake up time from this hibernation mode is greater than 1.0 second.

Table 26 defines at a high level one possible combination of hibernation mode configurations possible – refer to the data manual and respective application note for additional information.

**Table 26 Hibernation Mode Peripheral Status**

| Hibernation Mode Peripheral Status | | | |
|---|---|---|---|
| **Peripheral** | **Mode 1 Status** | **Mode 2 Status** | **Notes** |
| Debug Interface | OFF | OFF | |
| PCIe | ON | ON | |
| DDR3 | ON | ON | |
| MSMC SRAM | ON | OFF | |
| SRIO | ON | ON | |
| AIF | ON | ON | Can be multiple configurations |
| Accelerator(s) | ON | OFF | Refer to data manual for applicable accelerators |
| HyperLink | OFF | OFF | |
| FFTC | OFF | OFF | |
| Cores | INACTIVE | INACTIVE | Refer to application note and data manual for core status during stand by mode |
| SGMII | ACTIVE | ACTIVE | Can be multiple configurations |
| EMIF | ACTIVE | ACTIVE | |
| **End of Table 26** | | | |

## 9.3 Low Power Techniques

There exist multiple additional low power techniques that can be implemented in a design (depending on the use case). If the application requires multiple DSPs and can accommodate portioning of the DSPs such that certain DSPs can handle the bulk of the workload across defined periods of time – then the use of hibernation modes (identified above) is recommended.

In other use cases entire sections may be capable of powering down – making the application more "green." Selection of components including pull-up and pull-down resistor values and also reduce (or increase) current requirements on the power supplies. Power supply efficiency can be optimized through proper design and implementation.

## 9.4 General Power Saving & Design Techniques

The following provides a general overview of typical power saving techniques. Not all techniques apply for all applications. Consult the C66x device data manual for additional information.

- Generally, unused I/O pins should be configured as outputs and driven low to reduce ground bounce.
- Keep ground leads short, preferably tie individual ground pins directly to the respective ground plane.
- Eliminate pull-up resistors (where possible), or use pull-down resistors (where possible).
- The use of multi-layer PCBs that accommodate multiple separate power and ground planes take advantage of the intrinsic capacitance of GND-VCC plane topology and thus (when designed correctly) help to establish a better impedance board while utilizing the intrinsic capacitance inherent in the stack up design. A better matched impedance board will prevent less over and under shoots and / or reflections.

- Where possible, create synchronous designs that are not affected by momentarily switching pins.
- Keep traces connecting power pins stretching from power pins to a power plane (or island, or a decoupling capacitor) should be as wide and as short as possible. This reduces series inductance, and therefore, reduces transient voltage drops from the power plane to the power pin. Thus, reducing the possibility of ground bounce and coupled noise.
- Use high quality surface-mount low series resistance (ESR) capacitors to minimize the lead inductance. The capacitors should have an ESR value as small as possible. Ceramic capacitor should be used where possible.
- Use separate power planes for analog (PLL) power supplies (where possible).
- All PLL power supply planes should have a ground plane directly next to them in the stackup to minimize all power-generated noise.
- Where possible, place analog or digital components only over their respective ground planes.
- Connect each ground pin or via to the ground plane individually.
- Minimize the return current paths and inductance by not sharing vias with multiple ground pins.
- The use of the recommended filters will aid in isolating the PLL power from the digital power rails.
- Place as many bypass or decoupling capacitors as possible (minimum is the recommended amount), these should be placed between VCC and ground and be as short as possible. Ideally, the respective VCC pin should be tied directly to the decoupling capacitor which in turn should be tied directly to ground – this provides the shortest and lowest inductance path possible. If there must be a single trace connecting the decoupling capacitor to ground is should be between the VCC pin and the decoupling capacitor. If this is the case, then the trace between the device and decoupling capacitor must be as wide as the pin on the device (or wider where possible).
- Reduce the possible number of outputs that can switch at the same time (without impacting functionality).
- Sequence devices appropriately – especially during power up and power down. This will minimize crowbar and peak currents which in some cases could be a 50% increase over the initial design.
- The use of bigger vias (size) to connect the capacitor pads between power and ground planes aid in minimizing the overall inductance.

# 10 Simulation & Modeling

This section contains specific details pertaining to simulation and modeling.

Relevant documentation for Simulation and Modeling:

- KeyStone I Data Manual
- Using IBIS Models for Timing Analysis (SPRA839)

## 10.1 IBIS Modeling

Texas Instruments offers a fully validated standard IBIS model (IBIS 5.0 compliant) inclusive of all SerDes IO buffers. The available model will allow for full simulation using industry standard plug-in tools to such programs as Hyperlynx®. Because of the high performance nature of many of the KeyStone I IOs, the traditional IBIS model will also include embedded IBIS AMI models.

### 10.1.1 IBIS AMI Modeling

Given the performance requirements of many of today's input/output buffers, current IBIS models (IBIS 4.x compliant) are unable to properly characterize and produce results for many IOs operating above several hundred megahertz. For this reason the IBIS standard (4.x and previous) was modified (new revision 5.0 released Aug. 2008) incorporating the new AMI model.

AMI models (Algorithmic Modeling Interface) are black boxes which incorporate a unique parameter definition file which allows for specific data to be interchanged between EDA toolsets and standard models.

Texas Instruments is in the process of developing specific IBIS AMI models for the high performance SerDes and will be supported and released in the near future.

# 11 Appendix

This section contains additional and supporting information to be used during the design and integration of TI's C66x devices.

## 11.1 Phase Noise Plots

TI recommends specific clock types to be used in order to meet all clocking internal requirements. The following phase noise plots provided are for the CDCE62002 and CDCE62005 alternate clock sources. These clock sources are currently available for purchase and meet the needs of the device.

Figure 51 provides the Phase Noise data (plot) at 40 MHz. It is representative of both the CDC362002 and CDCE62005. This input frequency would be coupled to the DDR3 clock input of the device (provided the SDRAM were rated for 1.6 Gbps and the PLL multiplier was configured correctly).

**Figure 51 Phase Noise Plot - CECE62002/5 @ 40 MHz**

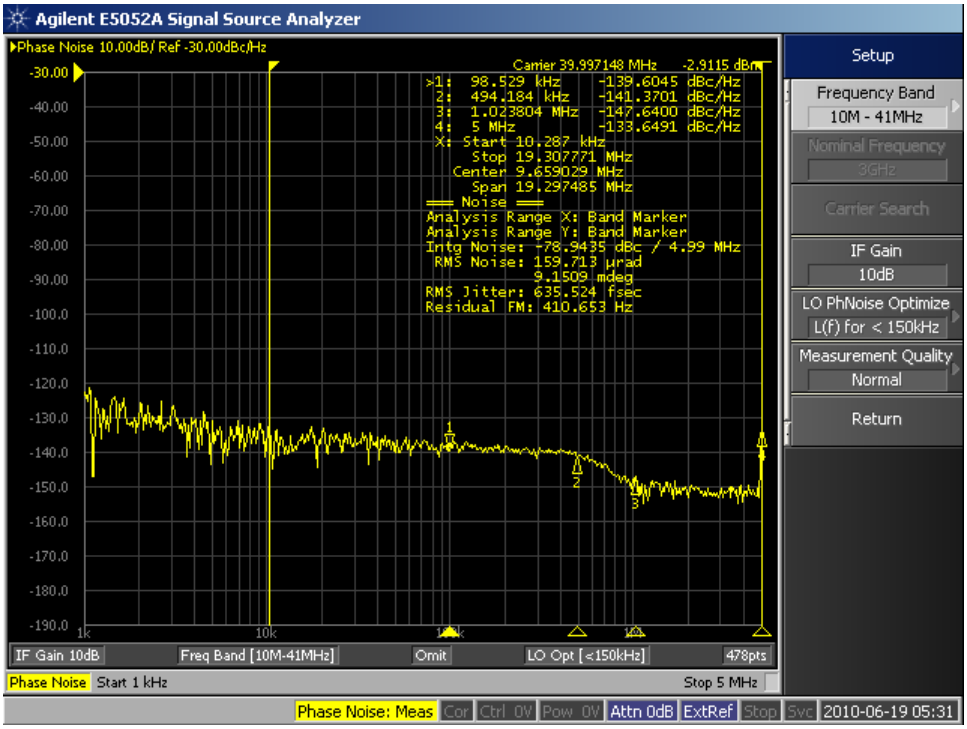


Figure 52 provides the Phase Noise data (plot) at 66.667 MHz. It is representative of both the CDC362002 and CDCE62005. This input frequency would be coupled to the DDR3 clock input of the device (provided the SDRAM were rated for 1.333 Gbps and the PLL multiplier was configured correctly).

**Figure 52 Phase Noise Plot - CECE62002/5 @ 66.667 MHz**

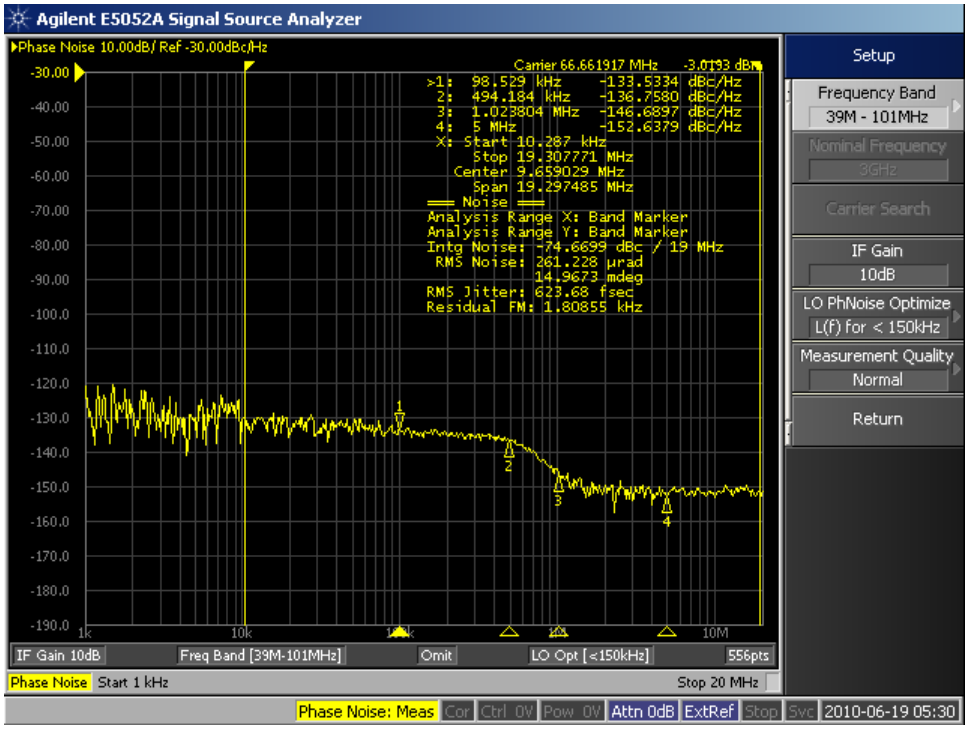


Figure 53 provides the Phase Noise data (plot) at 122.88 MHz. It is representative of both the CDC362002 and CDCE62005. This input frequency would be coupled to the ALTCORECLK or PASSCLK clock input of the device (provided this was the input frequency selected and the PLL multiplier was configured correctly).

**Figure 53 Phase Noise Plot - CECE62002/5 @ 122.88 MHz**

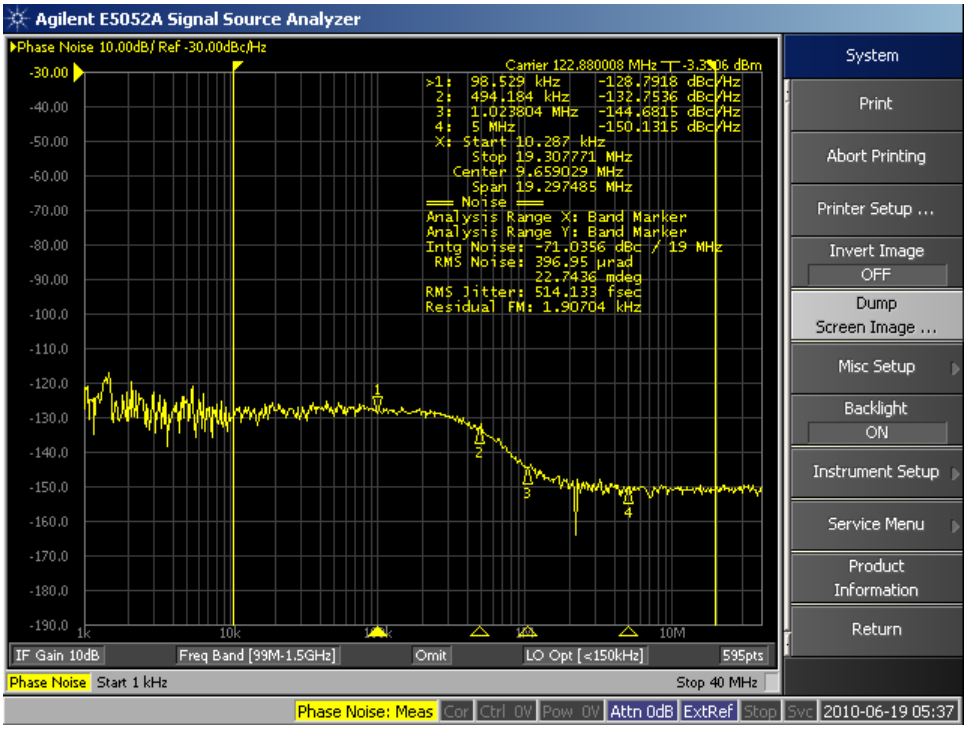


Figure 54 provides the Phase Noise data (plot) at 153.60 MHz. It is representative of both the CDC362002 and CDCE62005. This input frequency is intended to be coupled to the SYSCLK clock input of the device (provided this was the input frequency selected and the PLL multiplier was configured correctly). When visually overlaying this plot onto the previous SYSCLK plot we can see that we are below the maximum allowable mask input level to the device.

**Figure 54 Phase Noise Plot - CECE62002/5 @ 153.60 MHz**

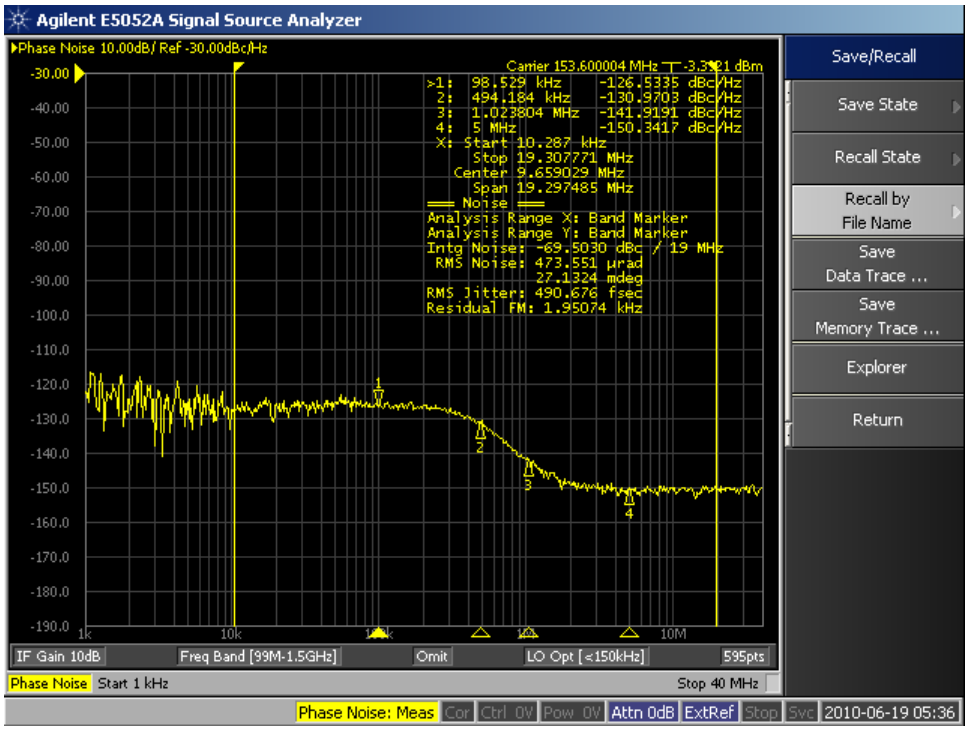


Figure 55 provides the Phase Noise data (plot) at 156.25 MHz. It is representative of both the CDC362002 and CDCE62005. This input frequency is intended to be coupled to the SRIO_SGMIICLK, PCIe_CLK, or MCMCLK clock input of the device (provided this was the input frequency selected and the PLL multiplier was configured correctly). When visually overlaying this plot onto the previous 156.25 MHz plot we can see that we are below the maximum allowable mask input level to the device.

**Figure 55 Phase Noise Plot - CECE62002/5 @ 156.25 MHz**

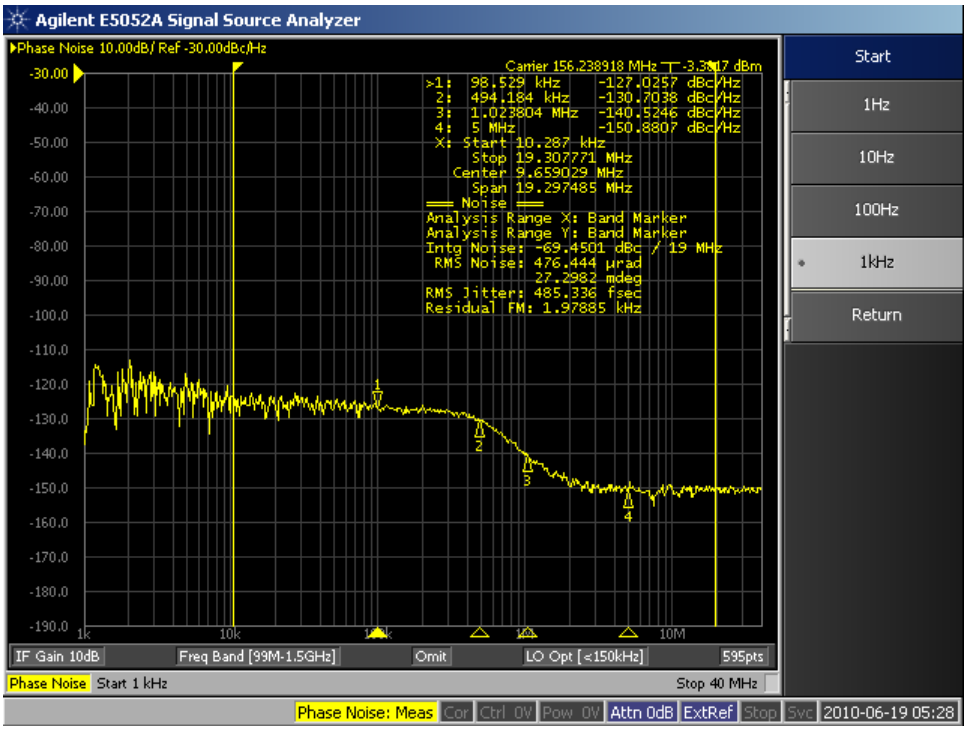
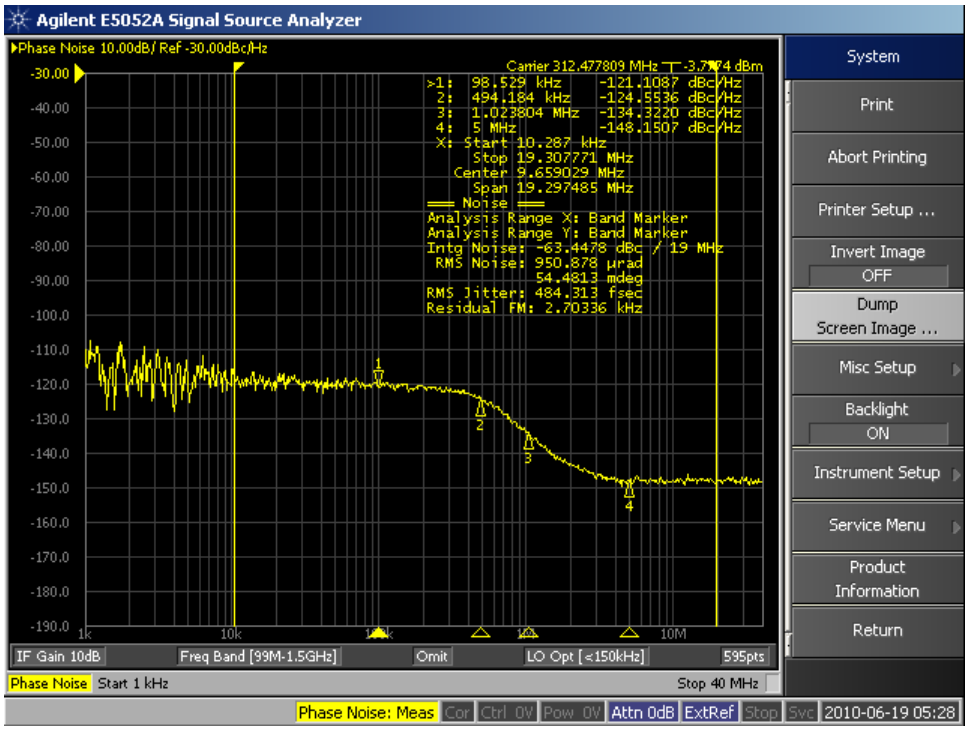


Figure 56 provides the Phase Noise data (plot) at 312.50 MHz. It is representative of both the CDC362002 and CDCE62005. This input frequency is recommended as the input clock for the SRIO_SGMIICLK, or MCMCLK clock into the device or as an alternate for the PCIe_CLK, ALTCORECLK, PASS_CLK,and DDR3CLK (to increase phase noise margins). Proper device configuration for this input clock frequency is mandatory. When visually overlaying this plot onto the previous 312.50 MHz plot we can see that we are below the maximum allowable mask input level to the device.

**Figure 56 Phase Noise Plot - CECE62002/5 @ 312.50 MHz**




## 11.2 Reflection Calculations

This section provides designers and engineers with an example of how to calculate, at a first approximation, the impact of a reflection. It does not take into account the magnitude or potential for cross-talk to a parallel signal.

Assumptions:

- Dielectric constant (Er) is 4.1
- Signal is routed internally and externally
- AC coupling capacitor is placed 250 mils (6.35mm) from the load
- Total net length is 3 inches (76.2mm)
- Frequency = 312.50MHz or 3.2ns period
- AC coupling capacitor size is 0402 and mounting pads meet IPC requirements

Calculations:

=85*SQRT((0.475*G13)+0.67) ==> results in the segment Tpd

As a first approximation, each segment was evaluated for Tpd (propagation delay) along a microstrip net. Each signal was further evaluated for the fundamental and secondary reflection (refer to Table 27). The individual segments highlighted in yellow denote which segments are the source of the potential reflection.

For the sake of this example, the period of the reflection is 30ps. However, this may not always be the case, which is where a simulation is beneficial.

These reflections (highlighted) would occur in the rising or falling edge of the clock periodic wave form. All others (refer to the Figure 57 timing analysis) would induce reflections, perturbations, or inflections during a logic 0 or logic 1 time frame and depending on magnitude could cause a logic transition, data error, or double clocking.

Reflections can occur at any point where an impedance mismatch occurs. The illustrations provided are only examples and are intended to illustrate the many possible permutations in a simple net that can occur (not all are comprehended in this example). For these reasons, simulation and modeling are always recommended.

**Table 27 Reflections in ps (Part 1 of 2)**

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **t0-t1** | **t1-t2** | **t2-t3** | **t3-t4** | **t4-t5** | | | | | | | | | | |
| | 2.7500 | 0.0350 | 0.0180 | 0.0350 | 0.2500 | | | | | | | | | | |
| | 378.1769 | 4.81316 | 2.47534 | 4.81316 | 34.37972 | | | | | | | | | | |
| reflection nodes | 378.1769 | 382.99 | 385.4654 | 390.2785 | 424.6582 | | | | | | | | | | |
| | | | | | | | | | | | | | | | |
| | **t0-t1** | **t1-t2** | **t2-t3** | **t3-ta2** | **ta2-ta3** | **ta3-ta4** | **ta4-ta5** | | | | | | | | |
| | 2.7500 | 0.0350 | 0.0180 | 0.0180 | 0.0180 | 0.0350 | 0.2500 | | | | | | | | |
| | 378.1769 | 4.81316 | **2.47534** | **2.47534** | **2.47534** | **4.81316** | **34.37972** | | | | | | | | |
| reflection nodes | 378.1769 | 382.99 | 385.4654 | 387.9407 | 390.4161 | 395.2292 | 429.6089 | | | | | | | | |
| | | | | | | | | | | | | | | | |
| | **t0-t1** | **t1-t2** | **t2-t3** | **t3-t4** | **t4-t5** | **t5-tb4** | **tb4-tb5** | | | | | | | | |
| | 2.7500 | 0.0350 | 0.0180 | 0.0350 | 0.2500 | 0.2500 | 0.2500 | | | | | | | | |
| | 378.1769 | 4.81316 | 2.47534 | 4.81316 | 34.37972 | **34.37972** | **34.37972** | | | | | | | | |
| reflection nodes | 378.1769 | 382.99 | 385.4654 | 390.2785 | 424.6582 | 459.038 | 493.4177 | | | | | | | | |
| | | | | | | | | | | | | | | | |
| | **tb0-tb1** | **tb1-tc0** | **tc0-tc1** | **tc1-tc2** | **tc2-tc3** | **tc3-tc4** | **tc4-tc5** | | | | | | | | |
| | 2.7500 | 2.7500 | 2.7500 | 0.0350 | 0.1800 | 0.0350 | 0.2500 | | | | | | | | |
| | 378.1769 | **378.1769** | **378.1769** | **4.81316** | **24.7534** | **4.81316** | **34.37972** | | | | | | | | |
| reflection nodes | 378.1769 | 756.3537 | 1134.531 | 1139.344 | 1164.097 | 1168.91 | 1203.29 | | | | | | | | |
| | | | | | | | | | | | | | | | |
| | **tb0-tb1** | **tb1-tc0** | **tc0-tc1** | **tc1-tc2** | **tc2-tc3** | **tc3-td2** | **td2-td3** | **td3-td4** | **td4-td5** | | | | | | |
| | 2.7500 | 2.7500 | 2.7500 | 0.0350 | 0.1800 | 0.0180 | 0.0180 | 0.0350 | 0.2500 | | | | | | |
| | 378.1769 | **378.1769** | **378.1769** | **4.81316** | **24.7534** | **2.47534** | **2.47534** | **4.81316** | **34.37972** | | | | | | |
| reflection nodes | 378.1769 | 756.3537 | 1134.531 | 1139.344 | 1164.097 | 1166.573 | 1169.048 | 1173.861 | 1208.241 | | | | | | |
| | | | | | | | | | | | | | | | |
| | **tb0-tb1** | **tb1-tc0** | **tc0-tc1** | **tc1-tc2** | **tc2-tc3** | **tc3-tc4** | **tc4-tc5** | **tc5-te4** | **te4-te5** | | | | | | |
| | 2.7500 | 2.7500 | 2.7500 | 0.0350 | 0.1800 | 0.0350 | 0.2500 | 0.2500 | 0.2500 | | | | | | |
| | 378.1769 | **378.1769** | **378.1769** | **4.81316** | **24.7534** | **4.81316** | **34.37972** | **34.37972** | **34.37972** | | | | | | |
| reflection nodes | 378.1769 | 756.3537 | 1134.531 | 1139.344 | 1164.097 | 1168.91 | 1203.29 | 1237.67 | 1272.049 | | | | | | |
| | | | | | | | | | | | | | | | |
| | **tb0-tb1** | **tb1-tc0** | **tc0-tc1** | **tc1-tc2** | **tc2-tc3** | **tc3-td2** | **td2-td3** | **td3-td4** | **td4-td5** | **td5-tf4** | **tf4-tf5** | | | | |
| | 2.7500 | 2.7500 | 2.7500 | 0.0350 | 0.1800 | 0.0180 | 0.0180 | 0.0350 | 0.2500 | 0.2500 | 0.2500 | | | | |
| | 378.1769 | **378.1769** | **378.1769** | **4.81316** | **24.7534** | **2.47534** | **2.47534** | **4.81316** | **34.37972** | **34.37972** | **34.37972** | | | | |
| reflection nodes | 378.1769 | 756.3537 | 1134.531 | 1139.344 | 1164.097 | 1166.573 | 1169.048 | 1173.861 | 1208.241 | 1242.62 | 1277 | | | | |

**Table 27 Reflections in ps (Part 2 of 2)**

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **te0-te1** | **te1-te2** | **te2-te3** | **te3-tf4** | **tf4-tg3** | **tg3-tg4** | **tg4-tg5** | | | | | | | | |
| | 2.7500 | 0.0350 | 0.0180 | 0.0350 | 0.0350 | 0.0350 | 0.2500 | | | | | | | | |
| | 378.1769 | **4.81316** | **2.47534** | **4.81316** | **4.81316** | **4.81316** | **34.37972** | | | | | | | | |
| reflection nodes | 378.1769 | 382.99 | 385.4654 | 390.2785 | 395.0917 | 399.9049 | 434.2846 | | | | | | | | |
| | | | | | | | | | | | | | | | |
| | **te0-te1** | **te1-te2** | **te2-te3** | **te3-tf2** | **tf2-tf1** | **tf1-tf0** | **tf0-tg1** | **tg1-tg2** | **tg2-tg3** | **tg3-th4** | **th4-th5** | | | | |
| | 2.7500 | 0.0350 | 0.0180 | 0.0180 | 0.0350 | 2.7500 | 2.7500 | 0.0350 | 0.0180 | 0.0350 | 0.2500 | | | | |
| | 378.1769 | **4.81316** | **2.47534** | **2.47534** | **4.81316** | **378.1769** | **378.1769** | **4.81316** | **2.47534** | **4.81316** | **34.37972** | | | | |
| reflection nodes | 378.1769 | 382.99 | 385.4654 | 387.9407 | 392.7539 | 770.9307 | 1149.108 | 1153.921 | 1156.396 | 1161.209 | 1195.589 | | | | |
| | | | | | | | | | | | | | | | |
| | **te0-te1** | **te1-te2** | **te2-te3** | **te3-tf4** | **tf4-tf3** | **tf3-tg2** | **tg2-th1** | **th1-tj2** | **tj2-tj3** | **tj3-tj4** | **tj4-tj5** | | | | |
| | 2.7500 | 0.0350 | 0.0180 | 0.0350 | 0.0350 | 0.0180 | 0.0350 | 0.0350 | 0.0180 | 0.0350 | 0.2500 | | | | |
| | 378.1769 | **4.81316** | **2.47534** | **4.81316** | **4.81316** | **2.47534** | **4.81316** | **4.81316** | **2.47534** | **4.81316** | **34.37972** | | | | |
| reflection nodes | 378.1769 | 382.99 | 385.4654 | 390.2785 | 395.0917 | 397.567 | 402.3802 | 407.1934 | 409.6687 | 414.4819 | 448.8616 | | | | |
| | | | | | | | | | | | | | | | |
| | **tk0-tk1** | **tk1-tk2** | **tk2-tk3** | **tk3-tf4** | **tk4-tk5** | **tk5-tl4** | **tl4-tl3** | **tl3-tl2** | **tl2-tl1** | **tl1-tl0** | **tl0-tm1** | **tm1-tm2** | **tm2-tm3** | **tm3-tm4** | **tm4-tm5** |
| | 2.7500 | 0.0350 | 0.0180 | 0.0350 | 0.2500 | 0.2500 | 0.0350 | 0.0180 | 0.0350 | 2.7500 | 2.7500 | **0.035** | **0.018** | **0.035** | **0.25** |
| | 378.1769 | **4.81316** | **2.47534** | **4.81316** | **34.37972** | **34.37972** | **4.81316** | **2.47534** | **4.81316** | **378.1769** | **378.1769** | **4.81316** | **2.47534** | **4.81316** | **34.37972** |
| reflection nodes | 378.1769 | 382.99 | 385.4654 | 390.2785 | 424.6582 | 459.038 | 463.8511 | 466.3265 | 471.1396 | 849.3165 | 1227.493 | 1232.307 | 1234.782 | 1239.595 | 1273.975 |

**End of Table 27**

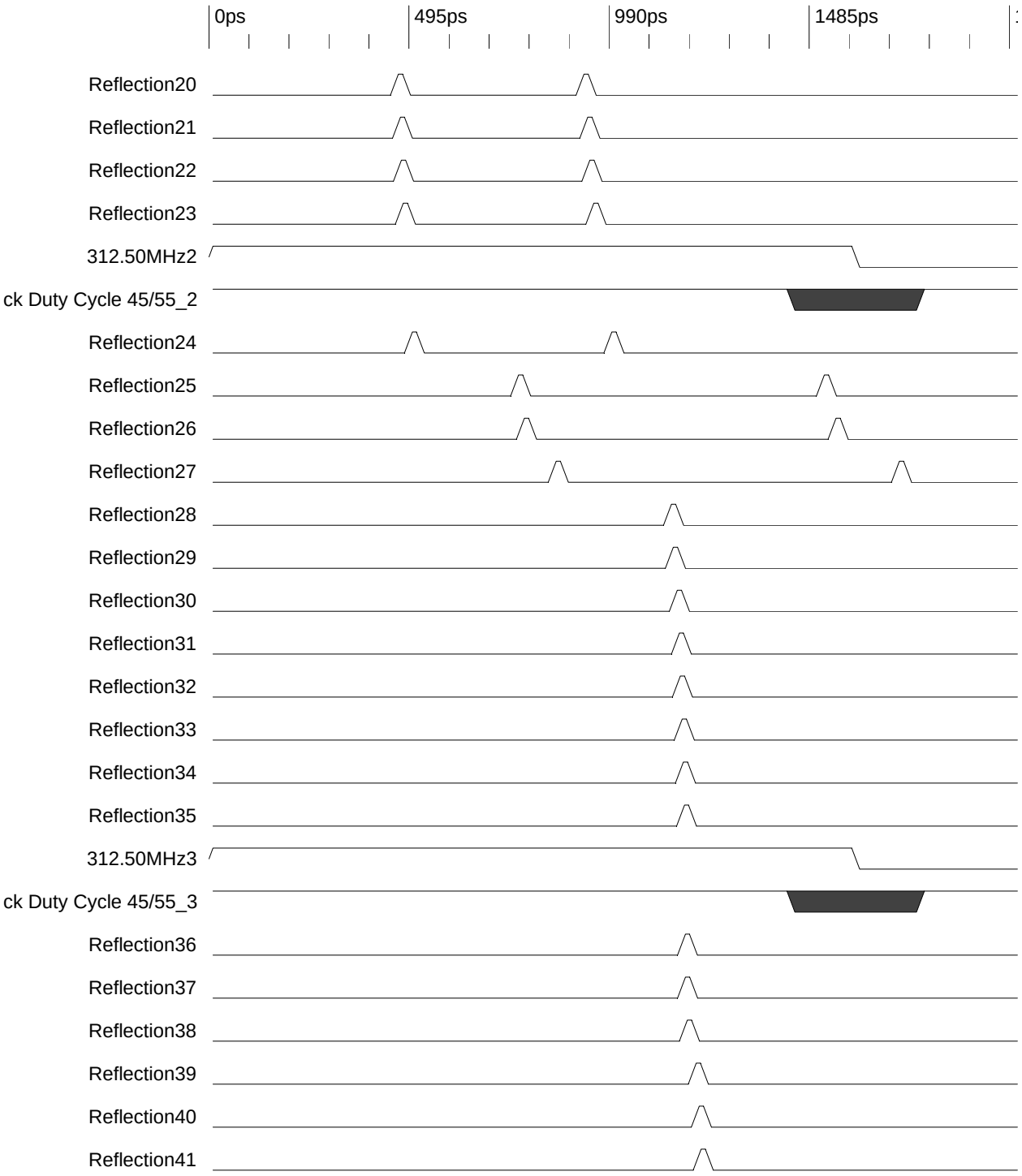
**Table 28 Possible First 50 Reflection Combinations (Part 1 of 2)**

| | Initial Reflections | | | Secondary Reflections | |
|---|---|---|---|---|---|
| # | Rising Edge | Falling Edge | | Rising Edge | Falling Edge |
| 1 | 0.3782 | 0.4082 | | 0.7564 | 0.7864 |
| 2 | 0.383 | 0.413 | | 0.766 | 0.796 |
| 3 | 0.3855 | 0.4155 | | 0.7709 | 0.8009 |
| 4 | 0.3879 | 0.4179 | | 0.7759 | 0.8059 |
| 5 | 0.3903 | 0.4203 | | 0.7806 | 0.8106 |
| 6 | 0.3904 | 0.4204 | | 0.7808 | 0.8108 |
| 7 | 0.3928 | 0.4228 | | 0.7855 | 0.8155 |
| 8 | 0.3951 | 0.4251 | | 0.7902 | 0.8202 |
| 9 | 0.3952 | 0.4252 | | 0.7905 | 0.8205 |
| 10 | 0.3976 | 0.4276 | | 0.7951 | 0.8251 |
| 11 | 0.3999 | 0.4299 | | 0.7998 | 0.8298 |
| 12 | 0.4024 | 0.4324 | | 0.8048 | 0.8348 |
| 13 | 0.4072 | 0.4372 | | 0.8144 | 0.8444 |
| 14 | 0.4097 | 0.4397 | | 0.8193 | 0.8493 |
| 15 | 0.4145 | 0.4445 | | 0.829 | 0.859 |
| 16 | 0.4247 | 0.4547 | | 0.8493 | 0.8793 |
| 17 | 0.4296 | 0.4596 | | 0.8592 | 0.8892 |
| 18 | 0.4343 | 0.4643 | | 0.8686 | 0.8986 |
| 19 | 0.4489 | 0.4789 | | 0.8977 | 0.9277 |
| 20 | 0.459 | 0.489 | | 0.9181 | 0.9481 |
| 21 | 0.4639 | 0.4939 | | 0.9277 | 0.9577 |
| 22 | 0.4663 | 0.4963 | | 0.9327 | 0.9627 |
| 23 | 0.4711 | 0.5011 | | 0.9423 | 0.9723 |
| 24 | 0.4934 | 0.5234 | | 0.9868 | 1.0168 |
| 25 | 0.7564 | 0.7864 | | 1.5127 | 1.5427 |
| 26 | 0.7709 | 0.8009 | | 1.5419 | 1.5719 |
| 27 | 0.8493 | 0.8793 | | 1.6986 | 1.7286 |
| 28 | 1.1345 | 1.1645 | | 2.2691 | 2.2991 |
| 29 | 1.1393 | 1.1693 | | 2.2787 | 2.3087 |
| 30 | 1.1491 | 1.1791 | | 2.2982 | 2.3282 |
| 31 | 1.1539 | 1.1839 | | 2.3078 | 2.3378 |
| 32 | 1.1564 | 1.1864 | | 2.3128 | 2.3428 |
| 33 | 1.1612 | 1.1912 | | 2.3224 | 2.3524 |
| 34 | 1.1641 | 1.1941 | | 2.3282 | 2.3582 |
| 35 | 1.1666 | 1.1966 | | 2.3331 | 2.3631 |
| 36 | 1.1689 | 1.1989 | | 2.3378 | 2.3678 |
| 37 | 1.169 | 1.199 | | 2.3381 | 2.3681 |
| 38 | 1.1739 | 1.2039 | | 2.3477 | 2.3777 |
| 39 | 1.1956 | 1.2256 | | 2.3912 | 2.4212 |
| 40 | 1.2033 | 1.2333 | | 2.4066 | 2.4366 |
| 41 | 1.2082 | 1.2382 | | 2.4165 | 2.4465 |
| 42 | 1.2275 | 1.2575 | | 2.455 | 2.485 |

**Table 28 Possible First 50 Reflection Combinations (Part 2 of 2)**

| | Initial Reflections | | | Secondary Reflections | |
|---|---|---|---|---|---|
| # | Rising Edge | Falling Edge | | Rising Edge | Falling Edge |
| 43 | 1.2323 | 1.2623 | | 2.4646 | 2.4946 |
| 44 | 1.2348 | 1.2648 | | 2.4696 | 2.4996 |
| 45 | 1.2377 | 1.2677 | | 2.4753 | 2.5053 |
| 46 | 1.2396 | 1.2696 | | 2.4792 | 2.5092 |
| 47 | 1.2426 | 1.2726 | | 2.4852 | 2.5152 |
| 48 | 1.272 | 1.302 | | 2.5441 | 2.5741 |
| 49 | 1.274 | 1.304 | | 2.5479 | 2.5779 |
| 50 | 1.277 | 1.307 | | 2.554 | 2.584 |
| **End of Table 28** | | | | | |

**Figure 57 Reflections Timing Analysis**



# 12 References

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2. OBSAI Reference Point 3 Specification, Version 4.1
3. OBSAI Reference Point 2 Specification, Version 2.1
4. OBSAI Reference Point 1 Specification, Version 2.1
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45. CDCE62002 - Four Output Clock Generator/Jitter Cleaner With Integrated Dual VCOs (SCAS882)
46. CDCE62005 - Five/Ten Output Clock Generator/Jitter Cleaner With Integrated Dual VCOs (SCAS862)
47. Common Trace Transmission Problems and Solutions (SPRAAK6)
48. Using xdsprobe with the XDS560 and XDS510 (SPRA758A)

# 13 Revision History

Table 29 lists the change history for this document.

**Table 29 Document Revision History**

| Revision | Comments |
|---|---|
| SPRABI2B | The table Maximum Device Compression - Leaded Solder Balls was updated. (Page 8)<br>The table Maximum Device Compression - Lead-Free Solder Balls was updated. (Page 8)<br>In the $\overline{\text{POR}}$ section, noted that: Most output signals will be disabled (high-impedance) while $\overline{\text{POR}}$ is low. (Page 9)<br>In the $\overline{\text{POR}}$ section, noted that: Power good logic can re-assert $\overline{\text{POR}}$ low when a power supply failure or brown-out occurs to prevent over-current conditions. (Page 9)<br>In the Device Reset section, reset modes information updated. (Page 9)<br>Added $\overline{\text{RESETFULL}}$ section. (Page 9)<br>Rewrite of the $\overline{\text{LRESET}}$ section. (Page 10)<br>In the $\overline{\text{RESET}}$ section, noted that $\overline{\text{RESET}}$ does not latch bootstrapping. (Page 10)<br>In the $\overline{\text{RESET}}$ section, noted that $\overline{\text{RESET}}$ is a software configurable function. (Page 10)<br>In the $\overline{\text{RESET}}$ section, noted that: When $\overline{\text{RESET}}$ is active low, all 3-state outputs are placed in a high-impedance state. (Page 10)<br>Reworked the Reset Implementation Considerations section. (Page 11)<br>Reworked the $\overline{\text{RESETSTAT}}$ section. (Page 12)<br>Statement added for multiple configuration inputs. (Page 12)<br>Updated references to HyperLink in the text that referred to it as HyperBridge or MCM. (Page 13)<br>Reworked the Boot Modes section. (Page 13)<br>Updated the "Managing Unused Clock Inputs" table. (Page 15)<br>In the Clocking Requirements table, added CORECLKp and CORECLKn. (Page 16)<br>Added CORECLK to the Clocking Requirements table. (Page 16)<br>Added CORECLK to the Clocking Requirements table. (Page 20)<br>Renamed the "Specific SerDes Input Clock Requirements" to "Reference Clock Jitter Requirements" and updated the content. (Page 24)<br>Added the Random Jitter section. (Page 24)<br>Updated Jitter information. (Page 24)<br>Updated the bulleted information points in the Clock Signal Routing section. (Page 29)<br>Added new section: 4.3.4 - HyperLink Net Classes & Specific Rules (Page 36)<br>In the Slew Rate Control table, corrected the "Setting" column. (Page 97)<br>Corrected the bits in the Setting column of the Slew Rate Control table. (Page 97) |
| SPRABI2A | Section 3.3.1: enhanced the information on Random and Deterministic jitter.<br>Section 5.7: updated note<br>Section 5.7.1: added new details<br>Section 5.7.1.1: added new details and a link<br>Section 7.2.4: changed pull up location from fixed core to variable core supply for HyperLink clock<br>Section 7.4.1: added reference to section 7.4.4 for RIOSGMIICLK<br>Section 7.4.4: changed pull up location from fixed core to CVDD core supply for SRIOSGMIISCLK<br>Section 7.5.3: changed pull up location from fixed core to CVDD core supply for SRIOSGMIISCLK<br>Section 7.6.3: changed pull up location from fixed core to CVDD core supply for PCIECLK<br>Section 7.8.4: changed pull up location from fixed core to CVDD core supply for DDR3CLK<br>Section 7.9.3: change to pull TRST low instead of high.<br>Added tables "Reflections in ps" on page 122 and "Possible First 50 Reflection Combinations" on page 124.<br>Throughout: Removed references to the CDCM6212 clocking part.<br>Added Table 3 to describe how unused clocks should be handled.<br>Section 2.5: Changed resistor value from 4.75k to 1k. |
| SPRABI2 | Initial release. |