HyperLink High Speed DSP Interface Core
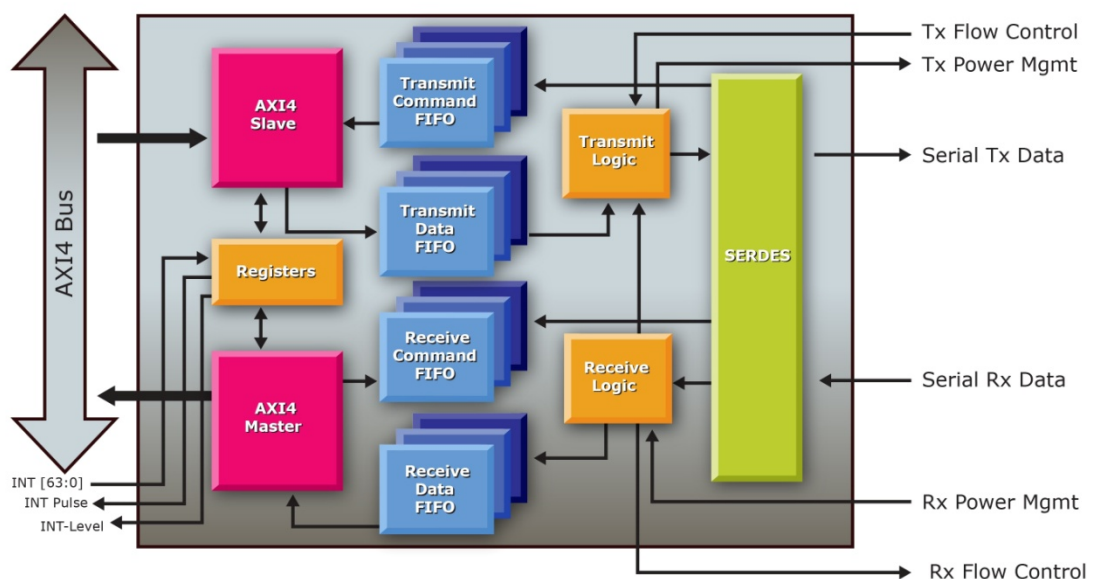
Open up your FPGA design to the power of the Texas Instruments DSP with the ***Integretek HyperLink High Speed DSP Interface Core***. The core provides a high speed, low pin count bi-directional interface connecting your FPGA design to a Texas Instruments C66X multi-core DSP.

25 Gbps Transfer Rate (4 lane)
Low Pin Count Interface
Industry Standard AXI Interface
Based on TI Proprietary Technology

FEATURES

- Up to 25Gbps transfer rate (4 lane) *
- SERDES data signals
- Dedicated LVCMOS pins for flow control and power management
- Point-to-point connection
- Link self-initializes
- Supports multiple outstanding read, write and interrupt transactions
- Simple packet-based transfer protocol for memory mapped access
- AXI4 Interface Complies with AMBA AXI Protocol V2.0
- Internal SERDES diagnostic loopback mode
- 64 user defined interrupt inputs, level and pulse sensitive

- AXI4 Slave (transmit to DSP and Control Register access)
  - 8,16,32,64,128 and 256 bit single cycle AXI accesses
  - 32,64,128 and 256 bit multi-beat AXI burst accesses
  - AXI INCR and WRAP Burst Types
  - Up to 16 outstanding write requests
  - Up to 16 outstanding read requests with unique read id's
  - AXI Private and Secure Access Types

- AXI4 Master (receive from DSP)
  - AXI INCR and WRAP Burst Types
  - Up to 16 outstanding read requests with unique read id's
  - AXI Private and Secure Access Types

BLOCK DIAGRAM

DELIVERABLES

The core package includes the following:

•Encrypted RTL
•Testbench and verification environment
•User Guide Documentation
•Compilation, simulation, and programming ready example project
•Technical Support

VERIFICATION

A Verilog environment is provided that includes:

•Testbench
•Sample Tests
     Tests represent typical use cases
•Adaptable to your application
•Scripts

WARRANTY and SUPPORT

The core as delivered is warranted against defect for one hundred days from purchase delivery date. Phone and Email product support is included for a period of thirty days. Optional product maintenance and support agreements are available.

ORDER INFORMATION

The HyperLink Interface core is available in the following configurations.

IP-HyperLink-A-S4 - Altera Stratix IV GX
IP-HyperLink-A-S5 - Altera Stratix V GX
IP-HyperLink-X-K7 - Xilinx Kintex 7
IP-HyperLink-X-V7 - Xilinx Virtex 7

Additional device families are being added, please check the Integre website for the latest device list.

COMPANION PRODUCTS

Integre offers the following products to assist with your HyperLink development:

FMC-950	HyperLink Connectivity Card With LVDS for FMC Platforms
HSMC-950	HyperLink Connectivity Card With LVDS for HSMC Platforms
IP-AXI-A/X	AXI DMA Controller for Altera/Xilinx
950-PLUG-LB	HyperLink Loopback Plug
IP-HyperLink-Maint	Twelve month IP Maintenance extension.

NOTES
*Future products slated for 50Gbps performance

All trademarks are property of their respective owners.